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Bloomington

CPU : INTEL PINEVIEW-M
 Chip Set : INTEL TIGERPOINT-M
 Remarks :

Model Name : PINE TRAIL-M
 PCB Part No : BA41-01184A
 BA41-01185A
 BA41-01186A
 Dev. Step : PV2
 Revision : 0.9
 T.R. Date : 2009.11.09

DRAW	CHECK	APPROVAL

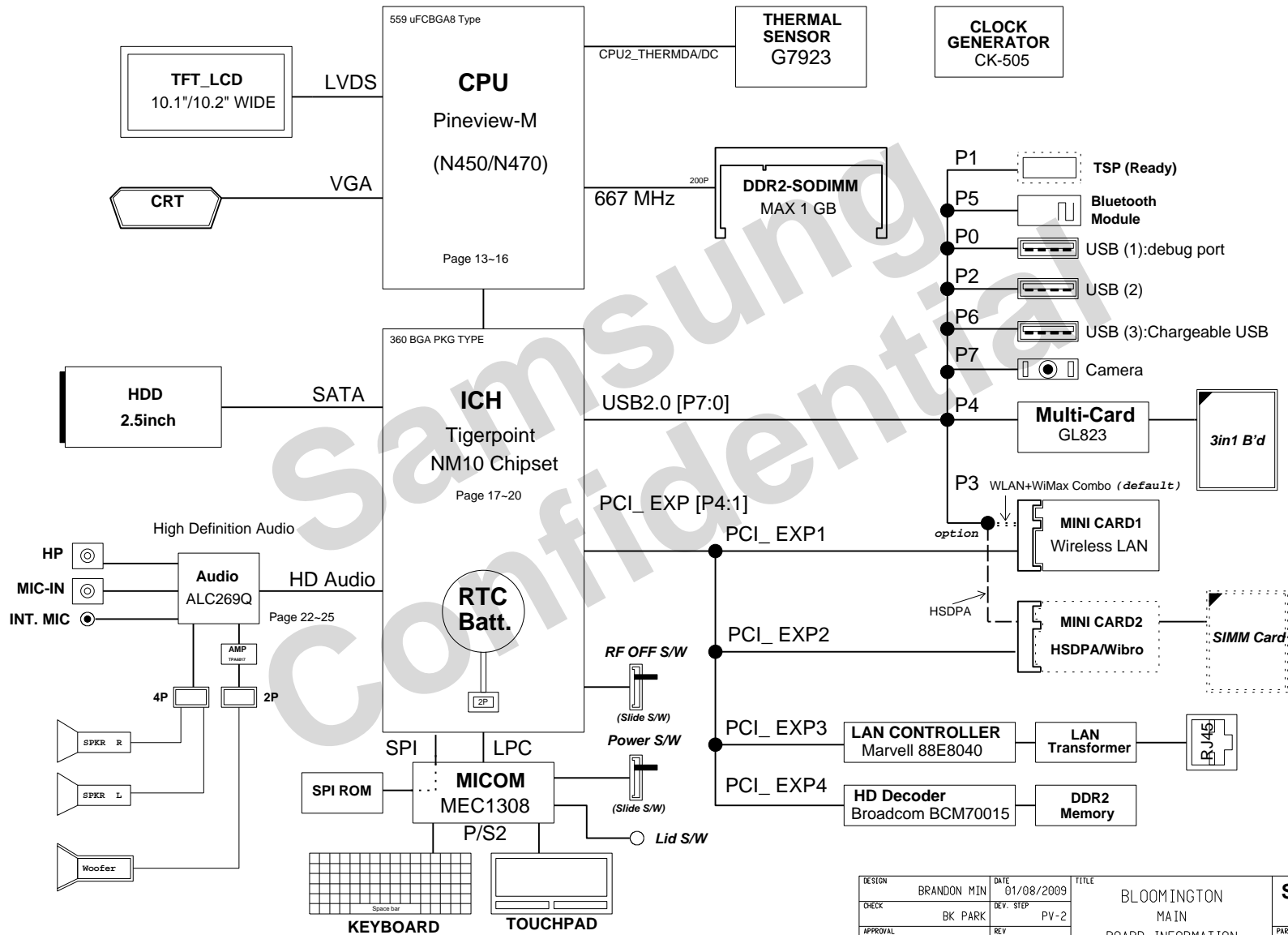
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DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON	SAMSUNG
CHECK	BK PARK	DEV. STEP	PV-2		MAIN	ELECTRONICS
APPROVAL	BJ LEE	REV	0.9		COVER	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	1	OF 43

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OPERATION BLOCK DIAGRAM



DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON MAIN	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2		BOARD INFORMATION	PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	2	OF 43

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BOARD INFORMATION**SCHEMATIC ANNOTATIONS AND BOARD INFORMATION****PCI Devices**

Devices	IDSEL#	REQ/GNT#	Interrupts
USB Hub to PCI LPC Bridge/IDE/AC97/SMBUS Internal MAC	AD29(internal) AD30(internal) AD31(internal) AD24(internal)	Programable	

Voltage Rails

Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Callistoga & ICH7-M
P3.3V_MICOM	3.3V always power rail(for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S3-S5)
P0.9V	0.9V power rail for DDR (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU

I²C / SMB Address

Devices	Address	Hex	Bus
ICH7M	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
CPU Thermal Sensor	0111 101X	7Ah	Thermal Sensor

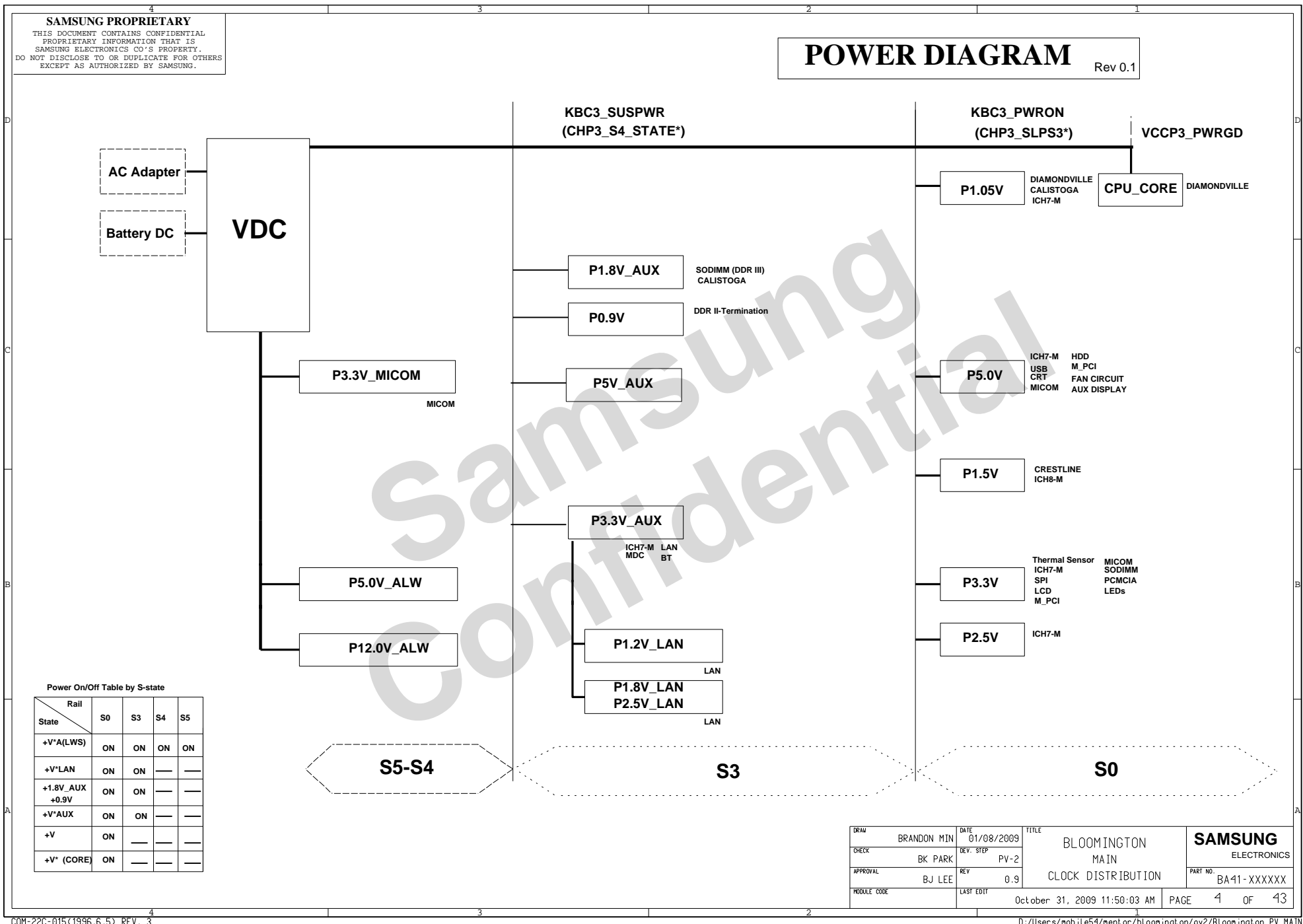
USB PORT Assign

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0 0	USB PORT	UHCL_2 4	USB PORT
UHCL_0 1	3-IN-1	UHCL_2 5	USB PORT
UHCL_1 2	Wireless LAN	UHCL_3 6	HSDPA
UHCL_1 3	BLUETOOTH	UHCL_3 7	CAMERA

PCI Express Assign

Port Number	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	Mini Card 2 (HSDPA/Wibro)
3	LOM

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CHECK	BK PARK	DEV. STEP	PV-2			PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	3	OF 43

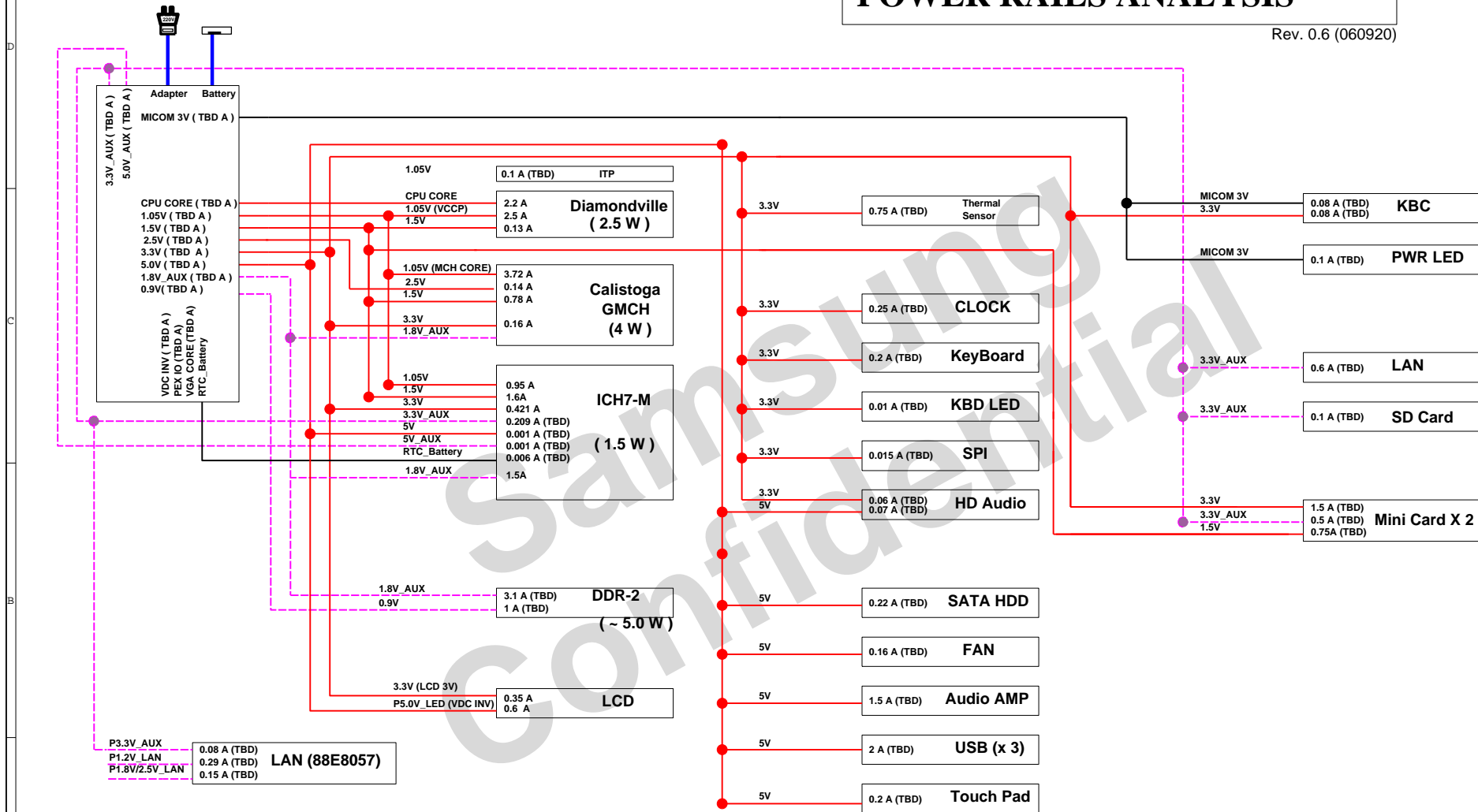


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POWER RAILS ANALYSIS

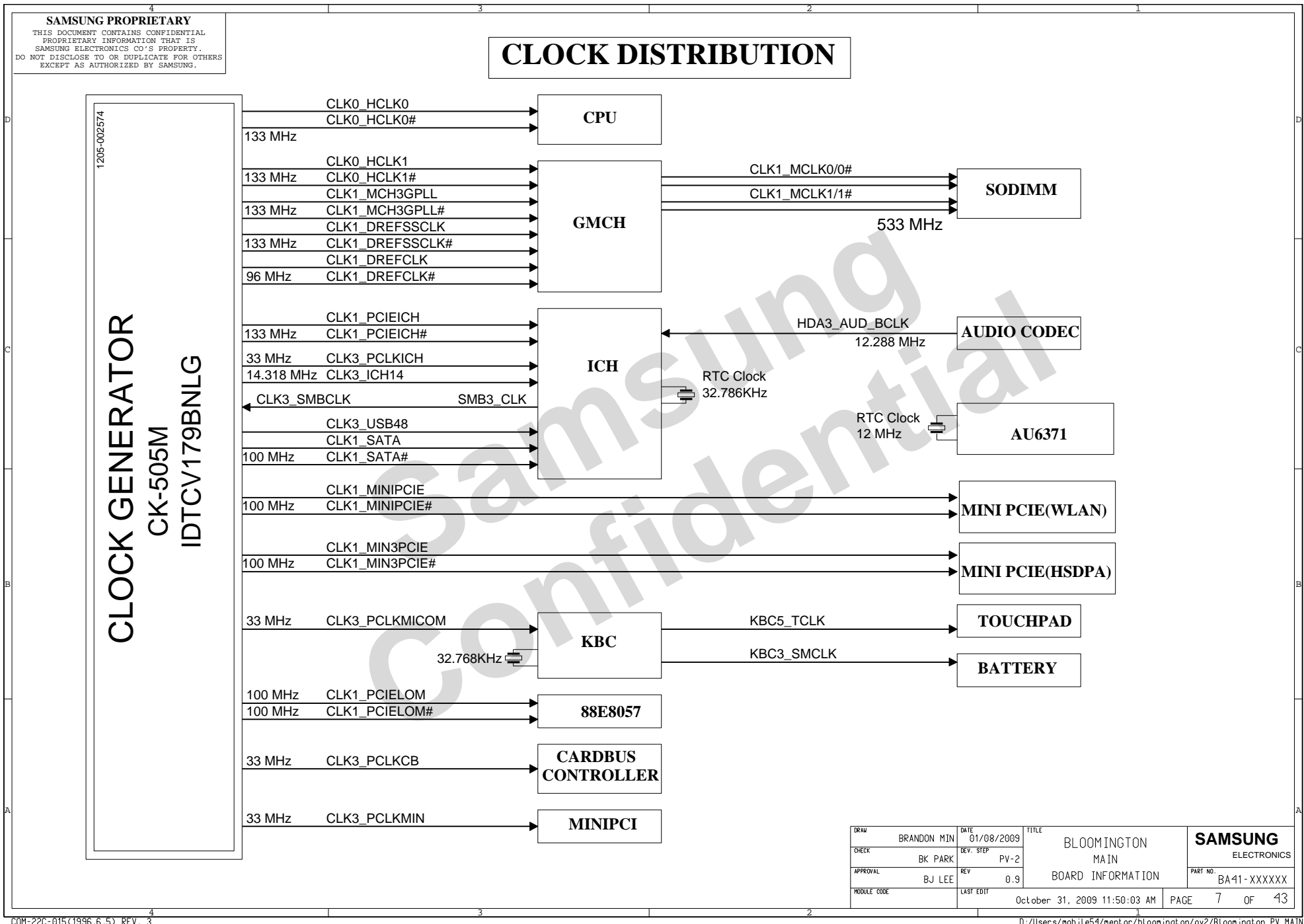
Rev. 0.6 (060920)



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APPROVAL	BJ LEE	REV	0.9	BOARD INFORMATION		PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	5	OF 43

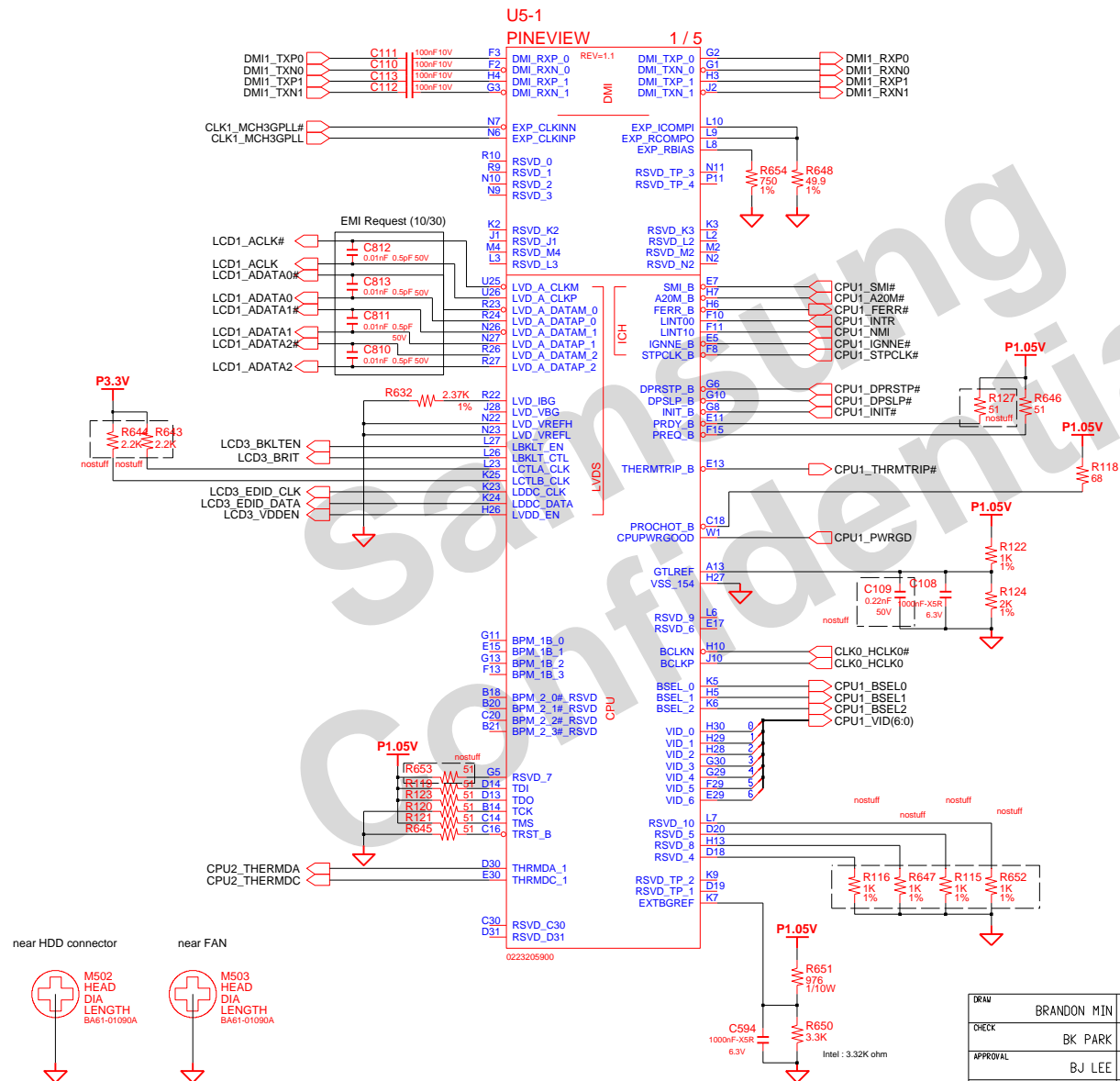
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PINEVIEW(1/3)

DRAW	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON CPU	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2		PINEVIEW (1/3)	PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	10	OF 43

U5-2 PINEVIEW 2/5

MEM1_AMA(0:14)

0	AH19	DDR_A_MA_0	DDR_A_DQS_0	AD3	0
1	AJ18	DDR_A_MA_1	DDR_A_DQS_1	AD8	1
2	AK18	DDR_A_MA_2	DDR_A_DQS_2	AD8	2
3	AJ14	DDR_A_MA_3	DDR_A_DQS_3	AK5	3
4	AH14	DDR_A_MA_4	DDR_A_DQS_4	AG22	4
5	AK14	DDR_A_MA_5	DDR_A_DQS_5	AE26	5
6	AJ12	DDR_A_MA_6	DDR_A_DQS_6	AE30	6
7	AH13	DDR_A_MA_7	DDR_A_DQS_7	AB27	7
8	AK12	DDR_A_MA_8			
9	AJ12	DDR_A_MA_9	DDR_A_DQS8_0	AD2	8
10	AK20	DDR_A_MA_10	DDR_A_DQS8_1	AD7	9
11	AH12	DDR_A_MA_11	DDR_A_DQS8_2	AD10	10
12	AJ11	DDR_A_MA_12	DDR_A_DQS8_3	AK3	11
13	AJ24	DDR_A_MA_13	DDR_A_DQS8_4	AG27	12
14	AJ10	DDR_A_MA_14	DDR_A_DQS8_5	AG27	13
			DDR_A_DQS8_6	AF29	14
			DDR_A_DQS8_7	AA27	15

MEM1_AWE#

MEM1_ACAS#

MEM1_ARAS#

MEM1_ABS0

MEM1_ABS1

MEM1_ABS2

MEM1_CS0#

MEM1_CS1#

MEM1_CKE0

MEM1_CKE1

MEM1_ODT0

MEM1_ODT1

CLK1_MCLK0

CLK1_MCLK0#

CLK1_MCLK1

CLK1_MCLK1#

P1.8V_AUX

ES1: Pull-up to +SM (WW10)

R673 10K

R672

R671 10K 1%

R689 10K 1%

R688 80.6 1%

C641 10nF

C640 100nF

R682 80.6 1%

DDR_A

MEM1_ADQS(7:0)

MEM1_ADQS#(7:0)

MEM1_ADM(7:0)

MEM1_ADQ(63:0)

DDR_A_DM_0

DDR_A_DM_1

DDR_A_DM_2

DDR_A_DM_3

DDR_A_DM_4

DDR_A_DM_5

DDR_A_DM_6

DDR_A_DM_7

DDR_A_DM_8

DDR_A_DM_9

DDR_A_DM_10

DDR_A_DM_11

DDR_A_DM_12

DDR_A_DM_13

DDR_A_DM_14

DDR_A_DM_15

DDR_A_DM_16

DDR_A_DM_17

DDR_A_DM_18

DDR_A_DM_19

DDR_A_DM_20

DDR_A_DM_21

DDR_A_DM_22

DDR_A_DM_23

DDR_A_DM_24

DDR_A_DM_25

DDR_A_DM_26

DDR_A_DM_27

DDR_A_DM_28

DDR_A_DM_29

DDR_A_DM_30

DDR_A_DM_31

DDR_A_DM_32

DDR_A_DM_33

DDR_A_DM_34

DDR_A_DM_35

DDR_A_DM_36

DDR_A_DM_37

DDR_A_DM_38

DDR_A_DM_39

DDR_A_DM_40

DDR_A_DM_41

DDR_A_DM_42

DDR_A_DM_43

DDR_A_DM_44

DDR_A_DM_45

DDR_A_DM_46

DDR_A_DM_47

DDR_A_DM_48

DDR_A_DM_49

DDR_A_DM_50

DDR_A_DM_51

DDR_A_DM_52

DDR_A_DM_53

DDR_A_DM_54

DDR_A_DM_55

DDR_A_DM_56

DDR_A_DM_57

DDR_A_DM_58

DDR_A_DM_59

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DDR_A_DM_81

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DDR_A_DM_87

DDR_A_DM_88

DDR_A_DM_89

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DDR_A_DM_93

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DDR_A_DM_99

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DDR_A_DM_110

DDR_A_DM_111

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DDR_A_DM_113

DDR_A_DM_114

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DDR_A_DM_139

DDR_A_DM_140

DDR_A_DM_141

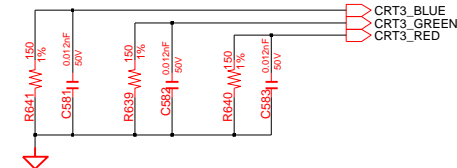
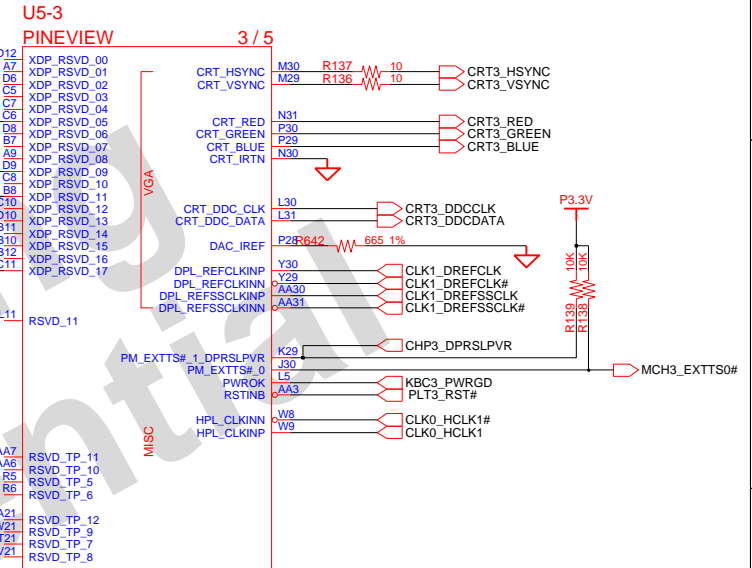
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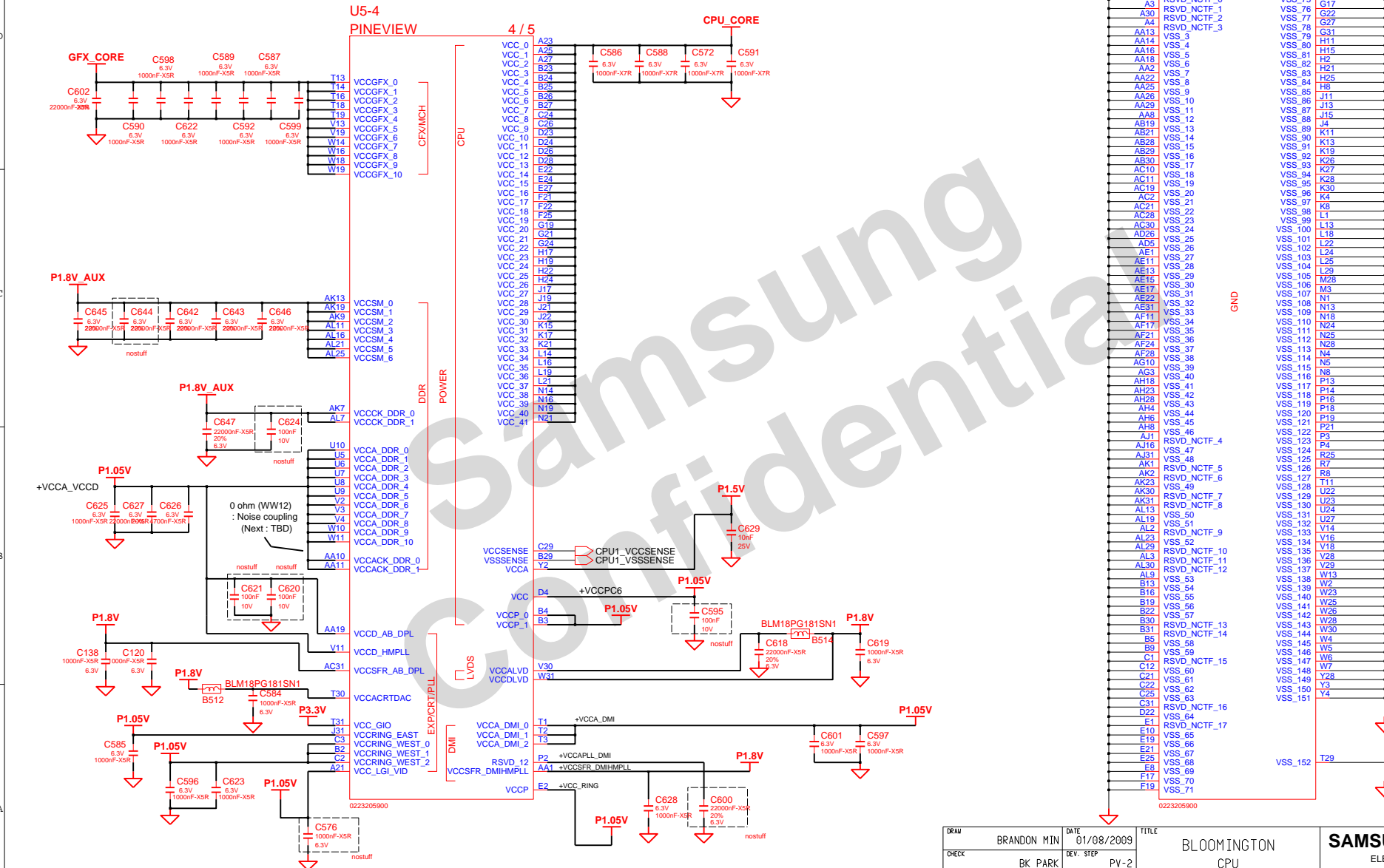


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CHECK BK PARK		REV. STEP PV-2				
APPROVAL BJ LEE		REV 0.9				
MODULE CODE		LAST EDIT October 31, 2009 11:50:03 AM				

U5-5

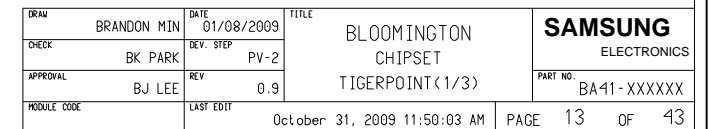
PINEVIEW

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DRAM	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON CPU PINEVIEW (3/3)	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE	LAST EDIT		October 31, 2009 11:50:03 AM			
					PART NO.	BA14-XXXXXX

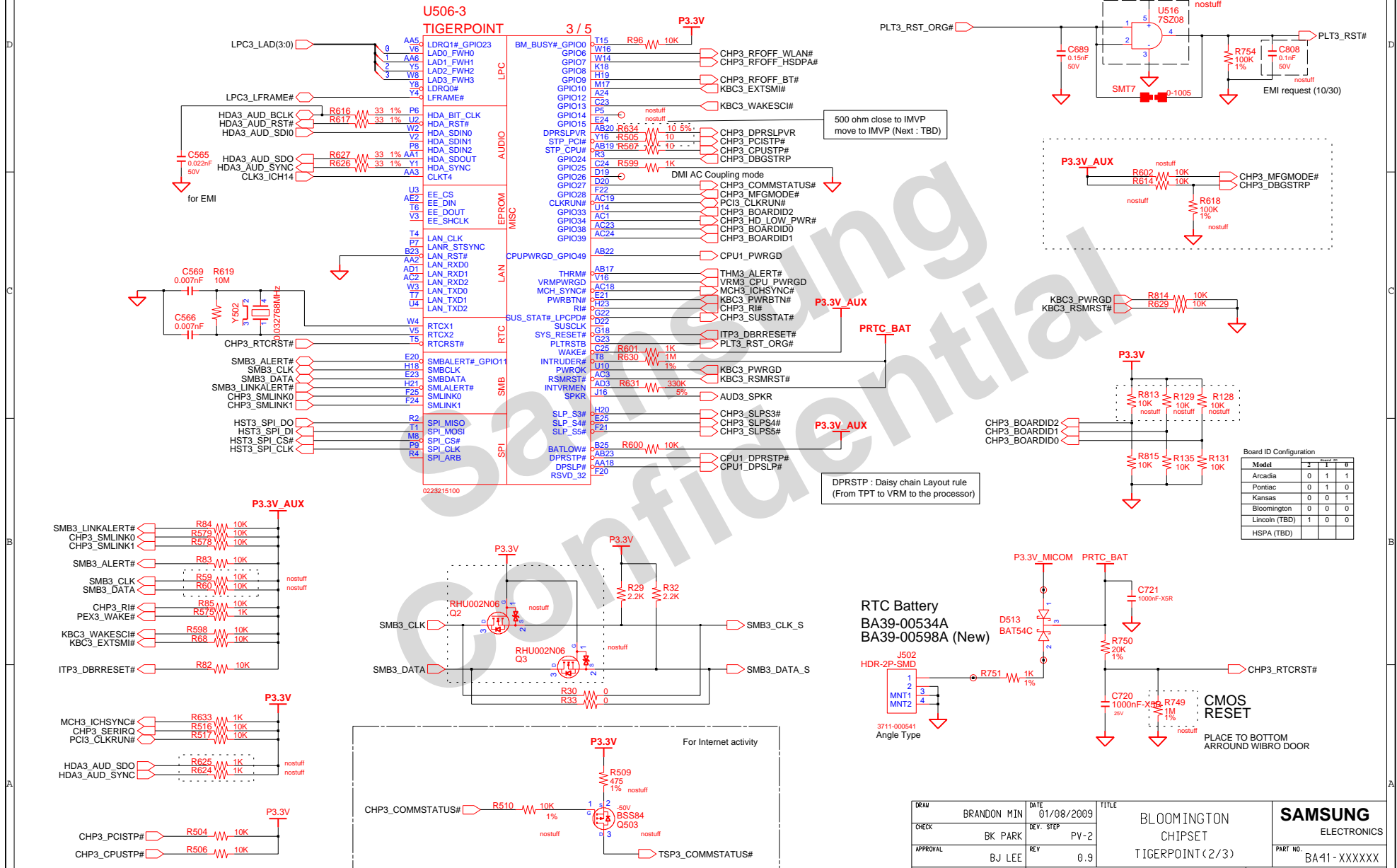
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Tigerpoint (2/3)

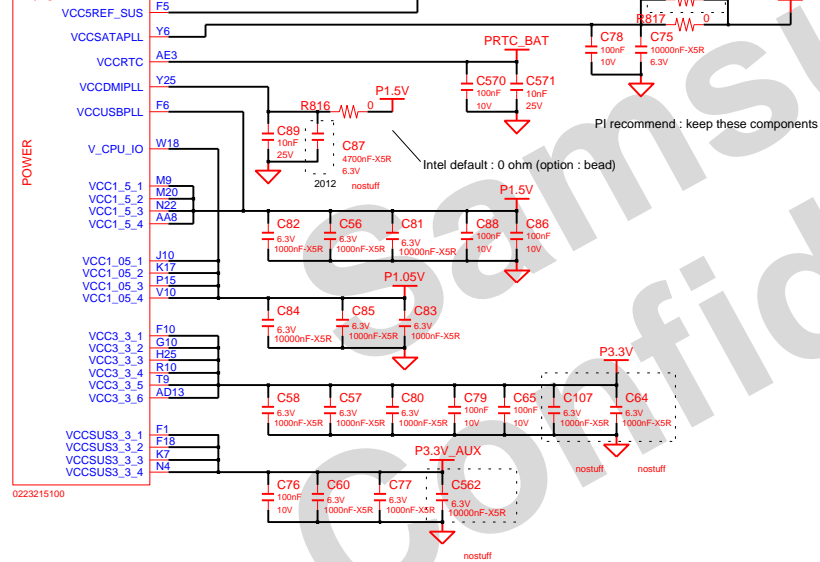


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Tigerpoint (3/3)**U506-4****TIGERPOINT**

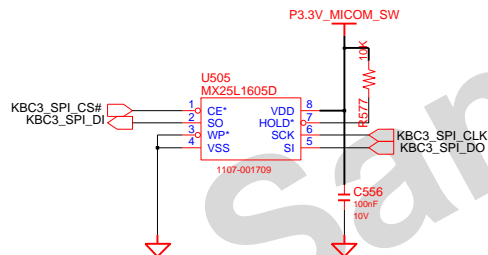
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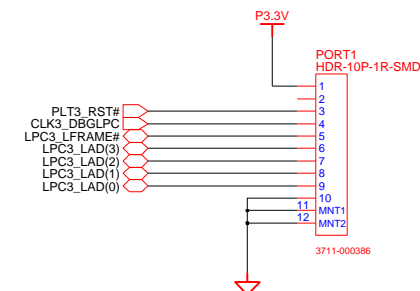
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SPI_BIOS_ROM



02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	78	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSOR IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	8E	SHADOW OPTION ROMS
18	8254 TIMER INIT	90	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	92	ENABLE H/W INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPUTE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B8	ACPI INIT
3D	LOAD ALTER REG. WITH CMOS VALUE	BA	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I2O SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	DE	ENABLE NMI
54	SET KEYCLICK IF ENABLED	E0	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	E2	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	E4	JUMP TO USER PATCH 2
5A	DISPLAY *PRESS SETUP*	E6	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 812K AND 640K	E8	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	EA	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

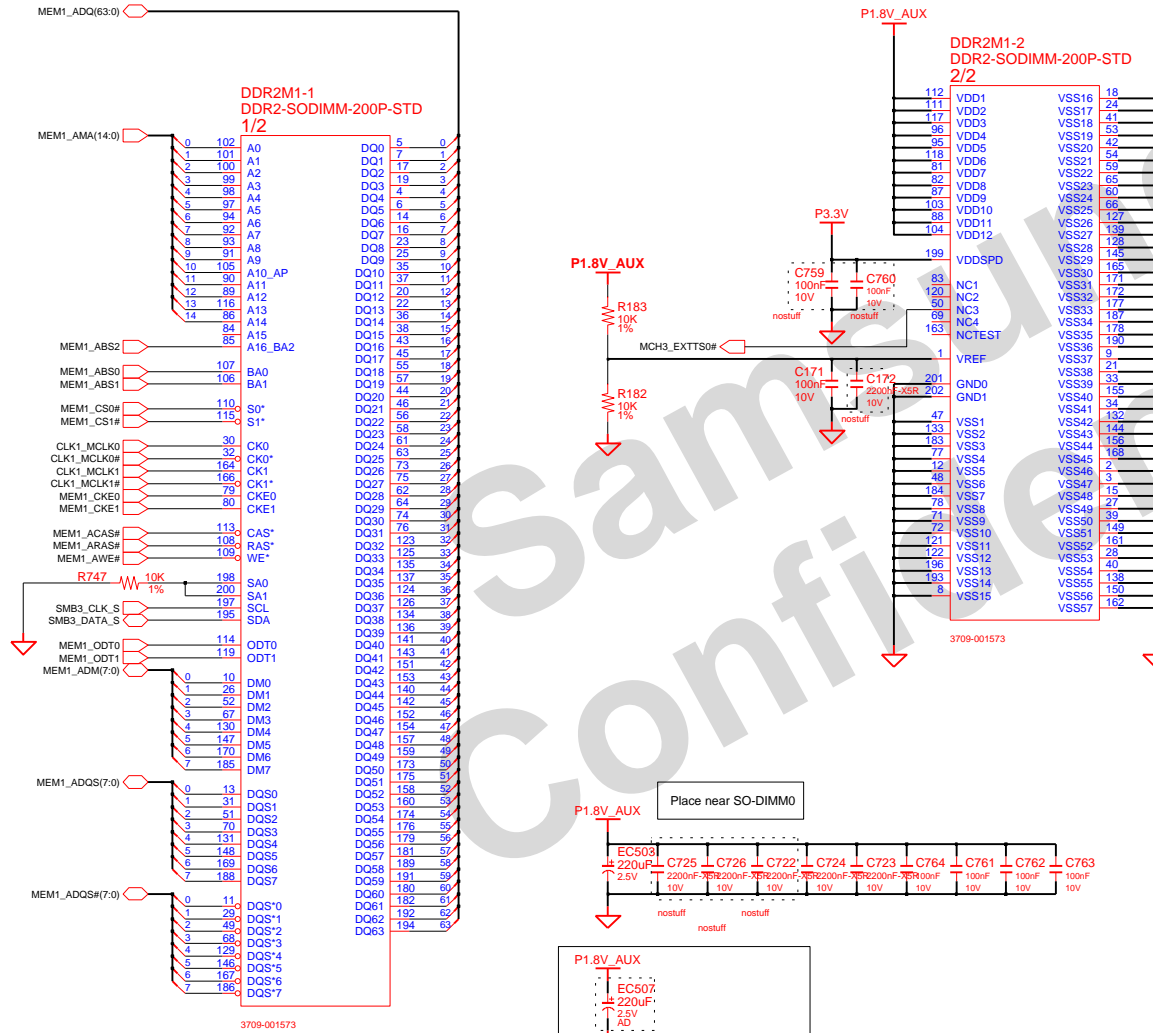
80H DECODER CONNECTOR



DRAW	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON	SAMSUNG
CHECK	BK PARK	DEV. STEP	PV-2		SPI_BIOS_ROM	ELECTRONICS
APPROVAL	BJ LEE	REV	0.9		SPI_BIOS_ROM	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	16	OF 43

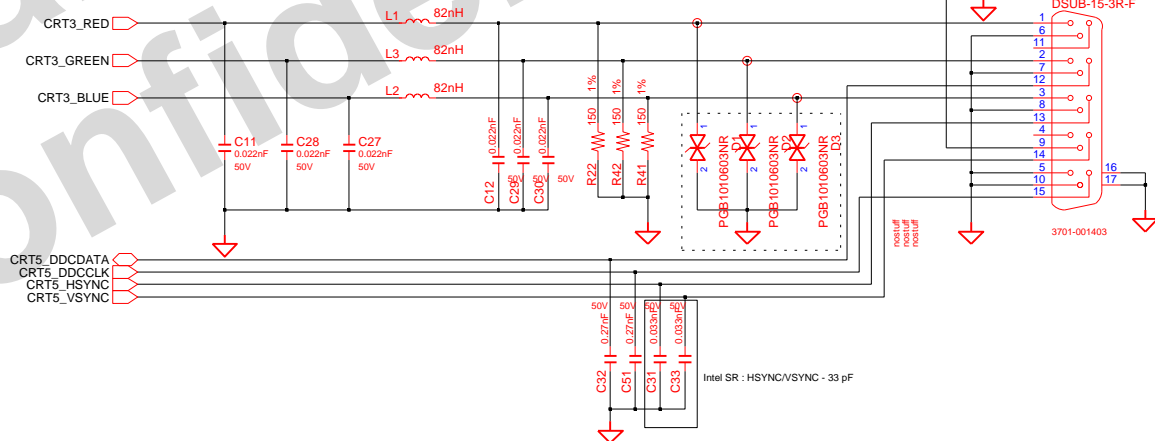
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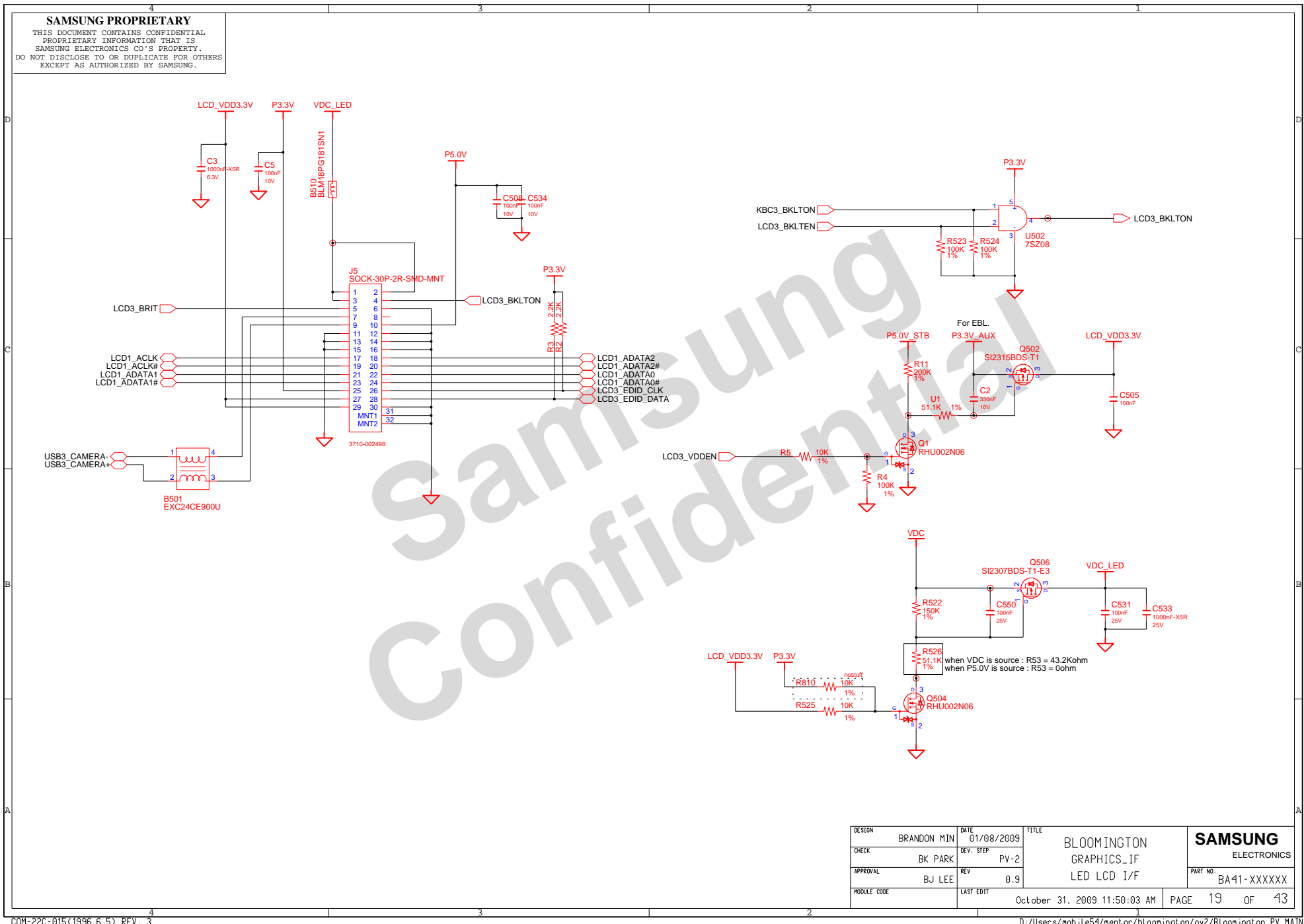
DDR SO-DIMM #0

DRAW	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON	SAMSUNG
CHECK	BK PARK	DEV. STEP	PV-2	SODIMM_DDR2	ELECTRONICS	
APPROVAL	BJ LEE	REV	0.9	SODIMM_DDR2 #1	PART NO.	BA41-XXXXXX
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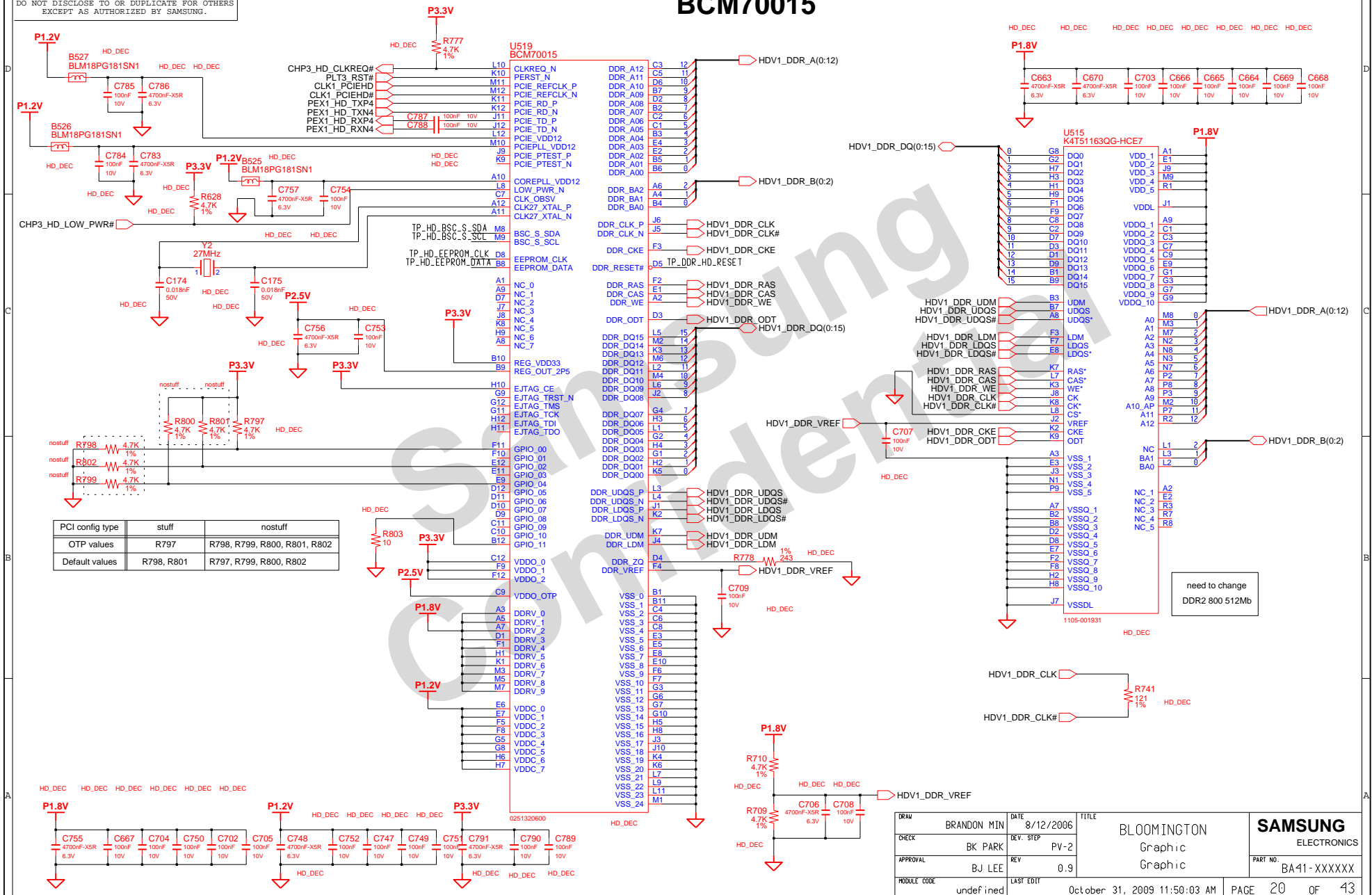
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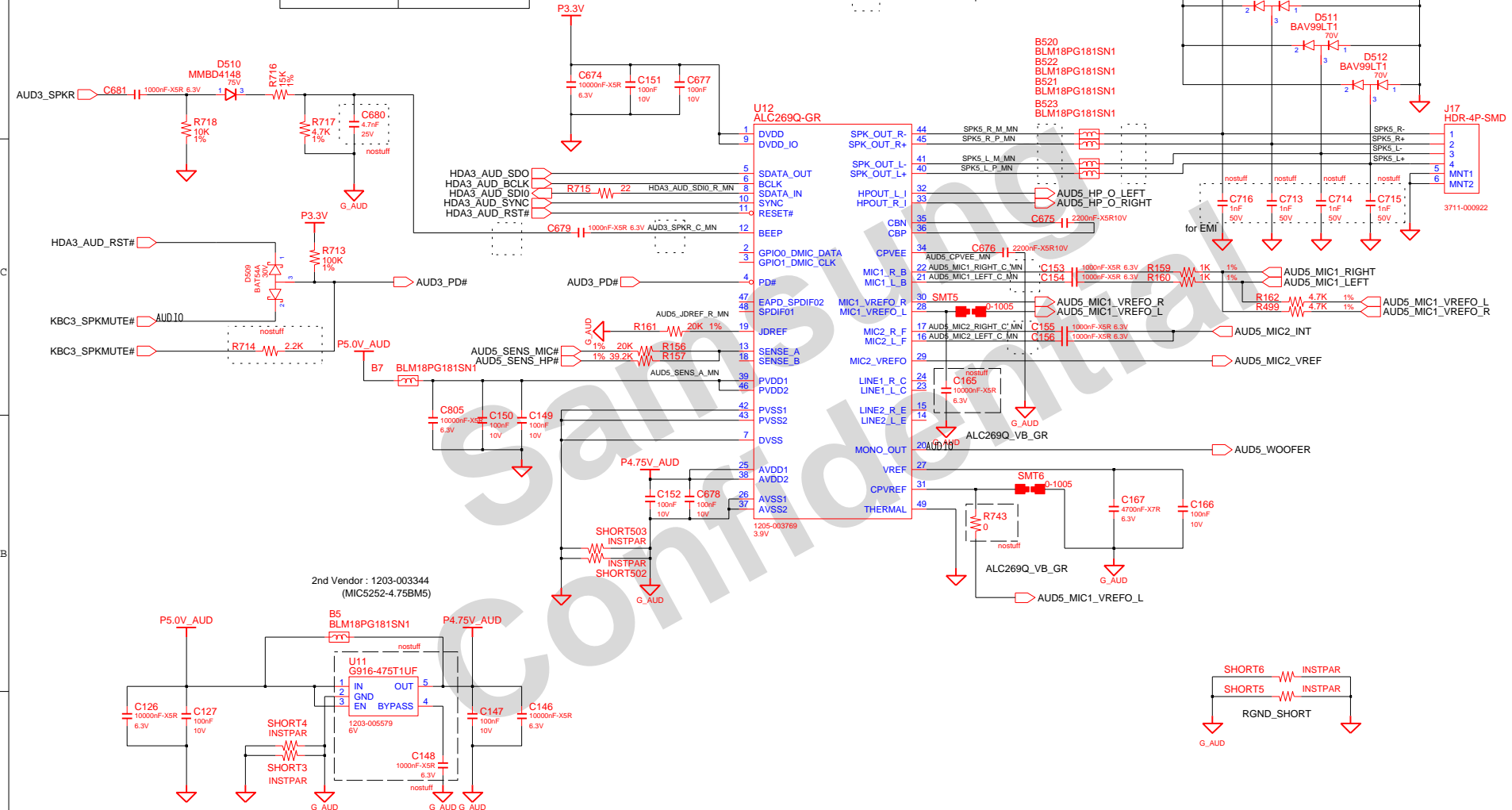
BCM70015

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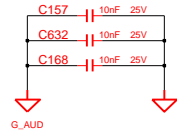
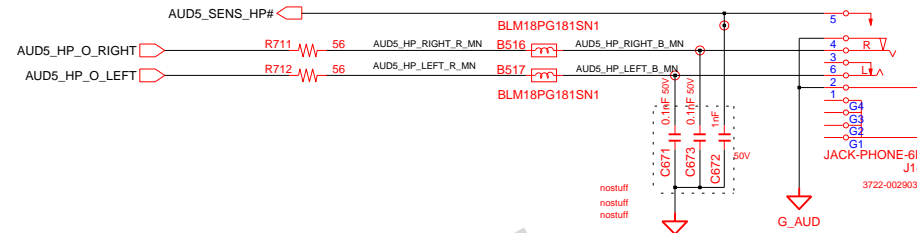
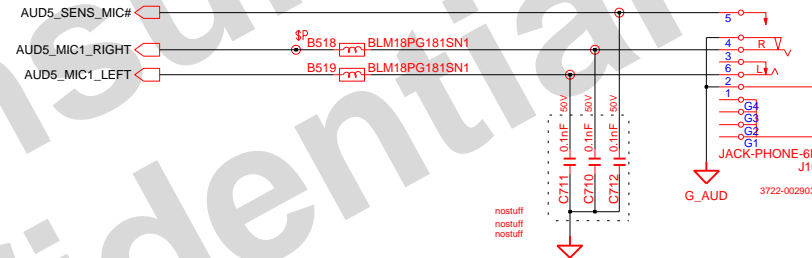
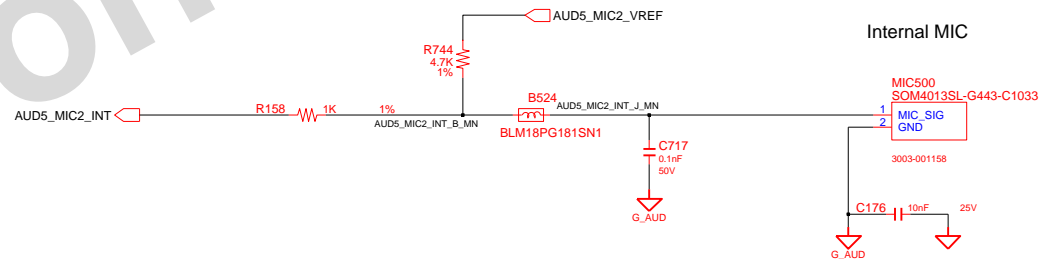
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE		BLOOMINGTON AUDIO AUDIO		SAMSUNG ELECTRONICS	
CHECK	BK PARK	REV. STEP	PV-2						
APPROVAL	BJ LEE	REV	0.9			PART NO.		BA11-XXXXXX	
MODULE CODE	LAST EDIT		October 31, 2009 11:50:03 AM			PAGE	21	OF	43

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**HEADPHONE****MIC JACK****Internal MIC**

DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON AUDIO AUDIO	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	23	OF 43

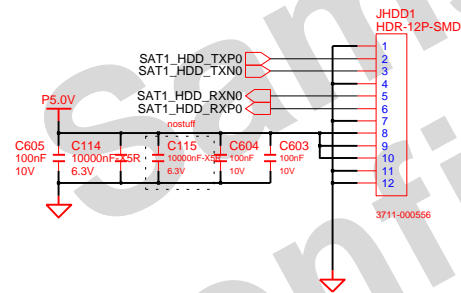
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APPROVAL	BJ LEE	REV	0.9		LAN		PART NO.	BA11-XXXXXX
MODULE CODE	LAST EDIT			October 31, 2009 11:50:03 AM	PAGE	24	OF	43

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SATA I/F CONN

SATA HDD CONN

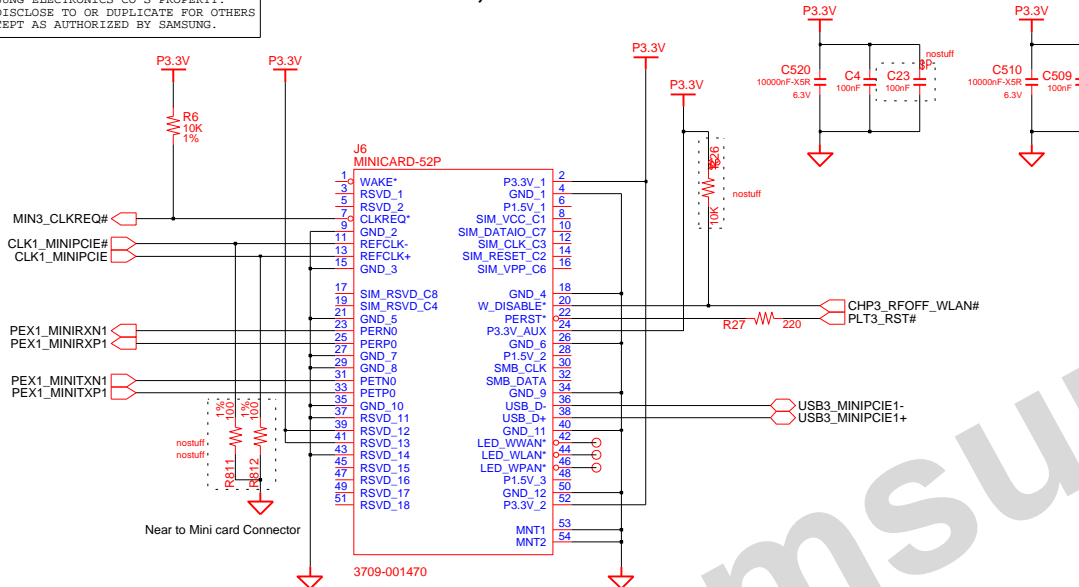


DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON SATA_DEVICES	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			
APPROVAL	BJ LEE	REV	0.9		SATA	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	25	OF 43

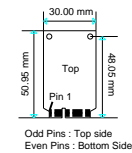
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WLAN, 5.2mm

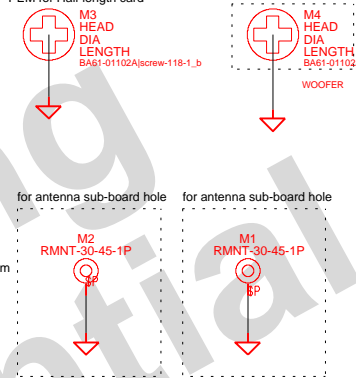


Mini PCI Express Card



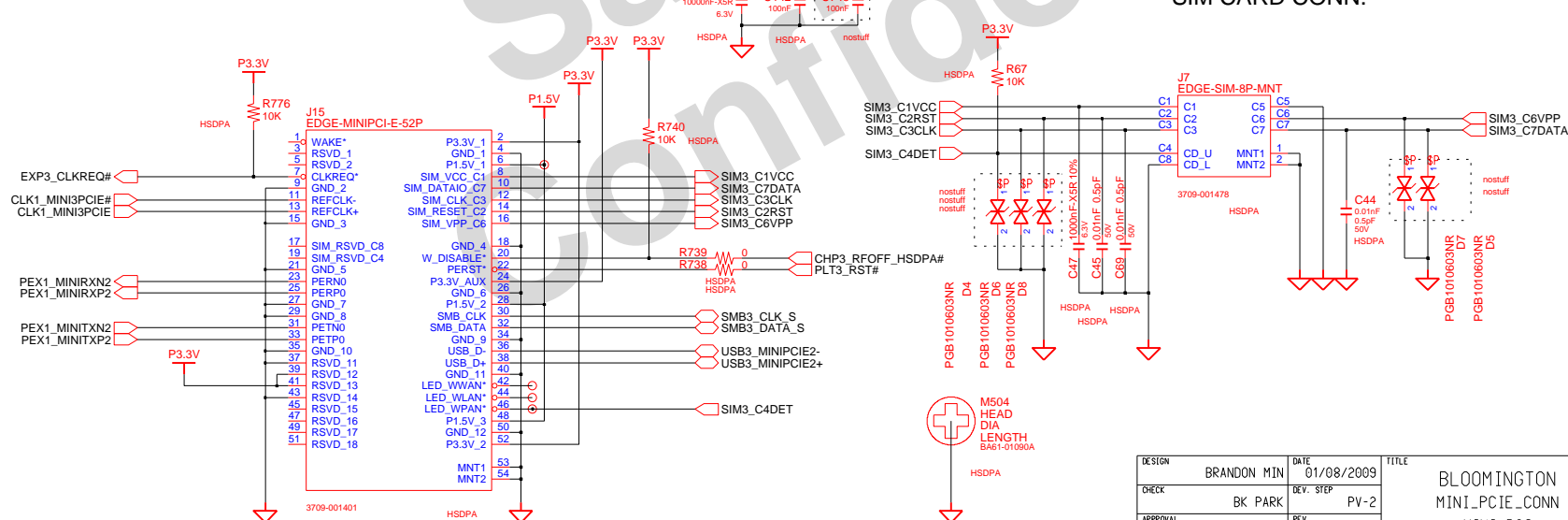
PEM for Half length card

Pontiac only

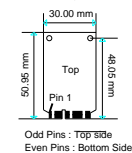


HSDPA / WIBRO, 4.0mm

SIM CARD CONN.



Mini PCI Express Card

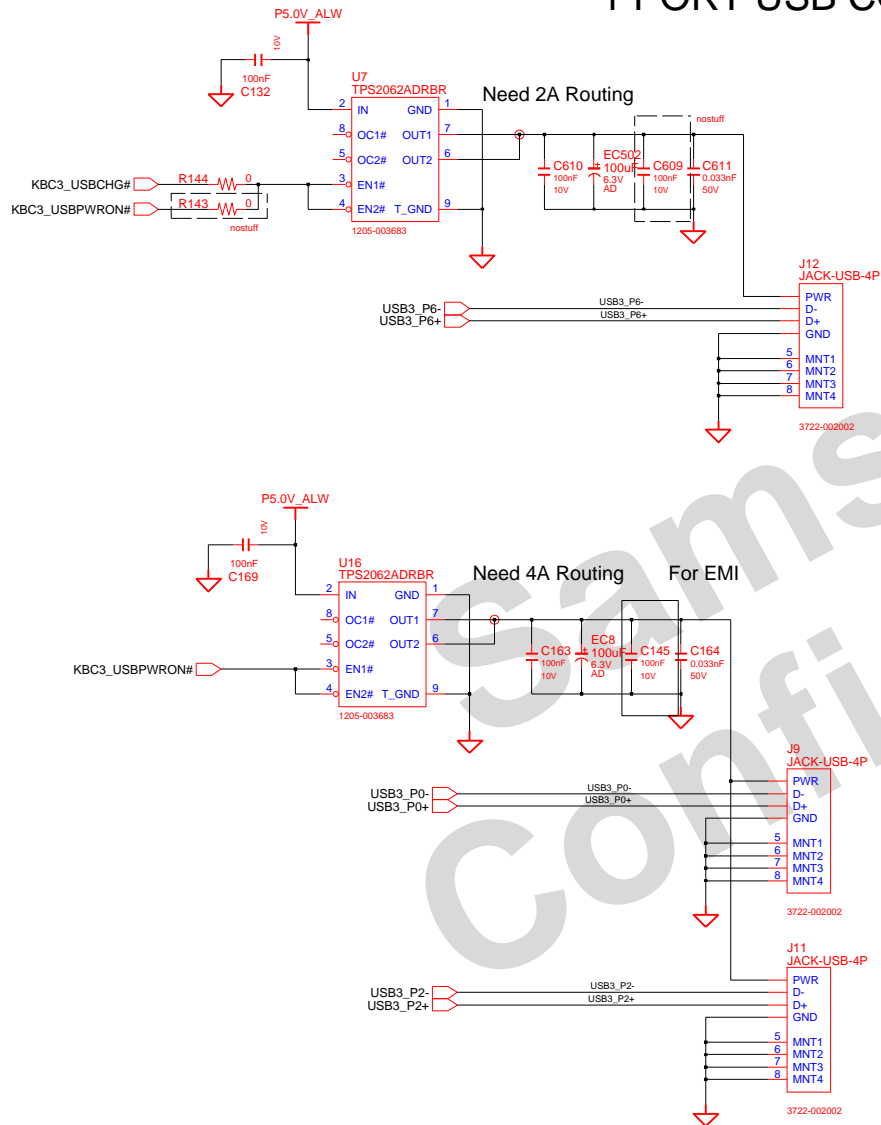
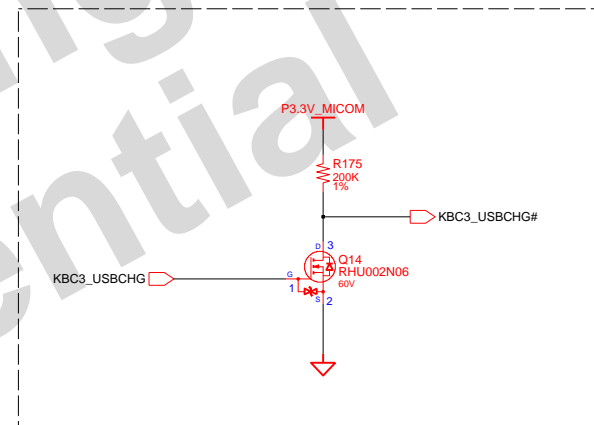


For SIM card Sub Board

DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON	SAMSUNG
CHECK	BK PARK	DEV. STEP	PV-2	MINI_PCIE_CONN	MINI PCI	ELECTRONICS
APPROVAL	BJ LEE	REV	0.9			PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	26	OF 43

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1 PORT USB CONNECTOR**Chargeable USB**

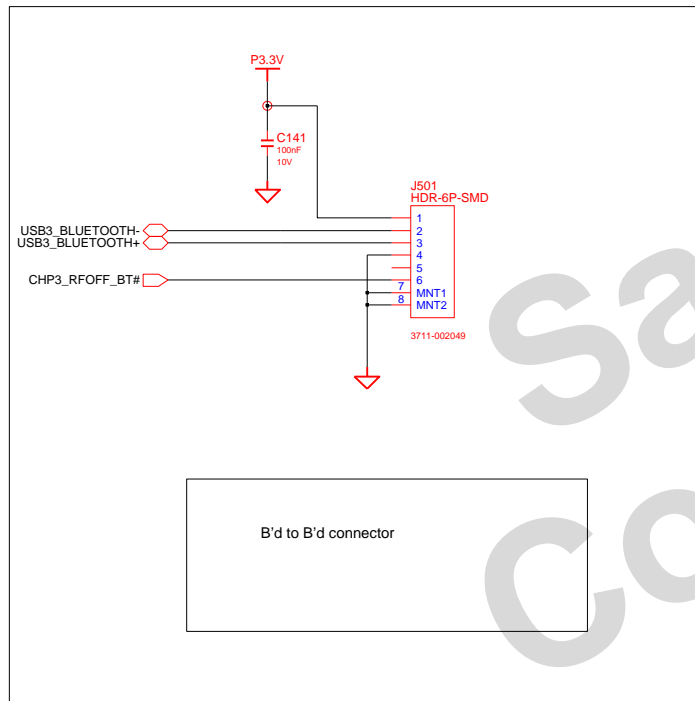
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APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	27	OF 43

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USB I/F Devices

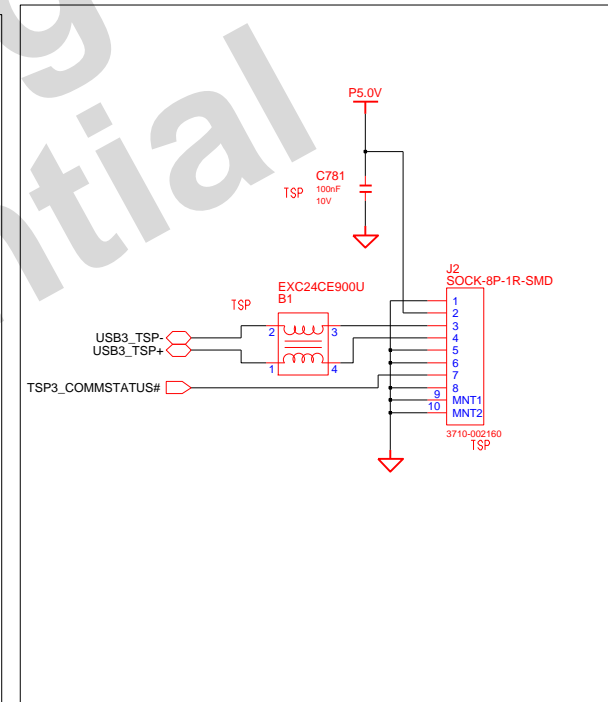
Bluetooth Interface



CAMERA

Camra I/F Circuit was moved to LVDS I/F Circuit Block.

TSP(Only for Lincon Model)

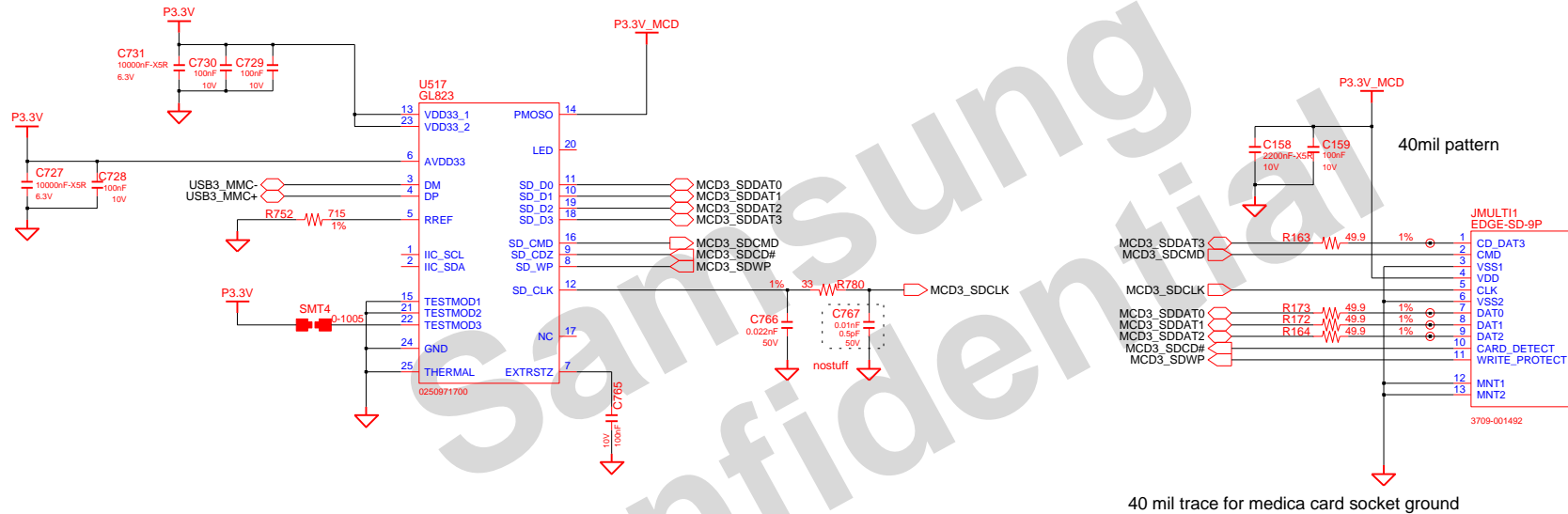


DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON USB_DEVICES BLUETOOTH CAMERA	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	28	OF 43

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MMC(GL823)



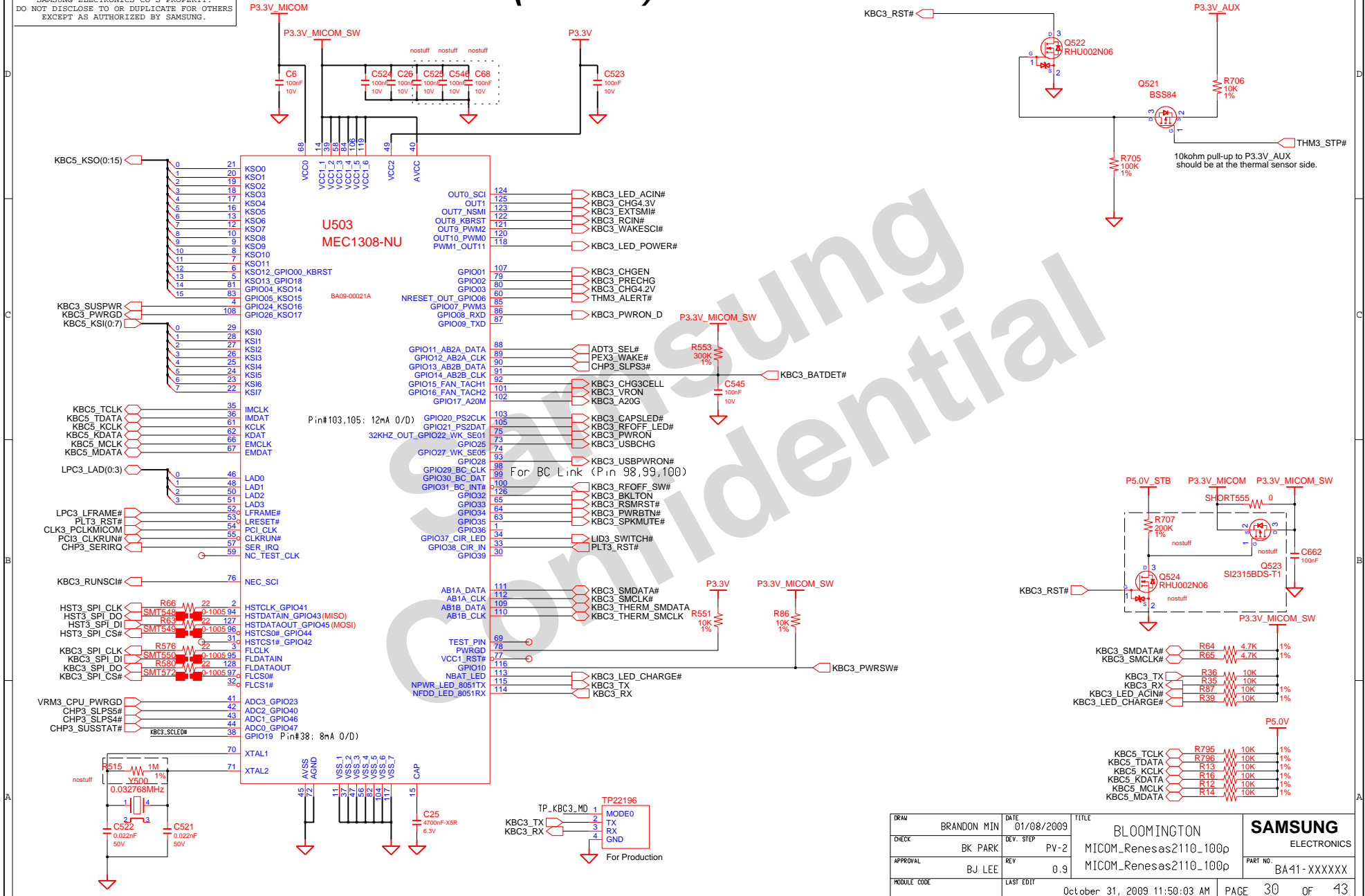
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CHECK	BK PARK	DEV. STEP	PV-2			PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	15	unmodified

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MAIN BOARD (MICOM)

MICOM RESET

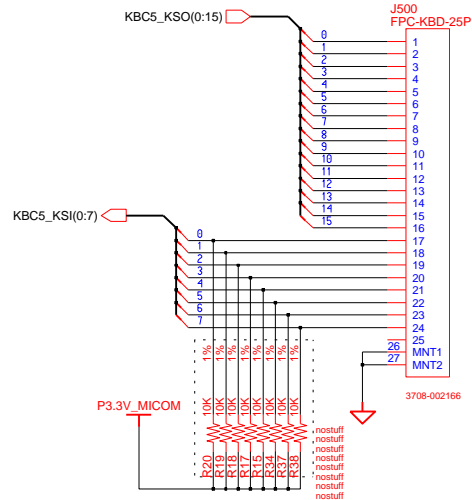


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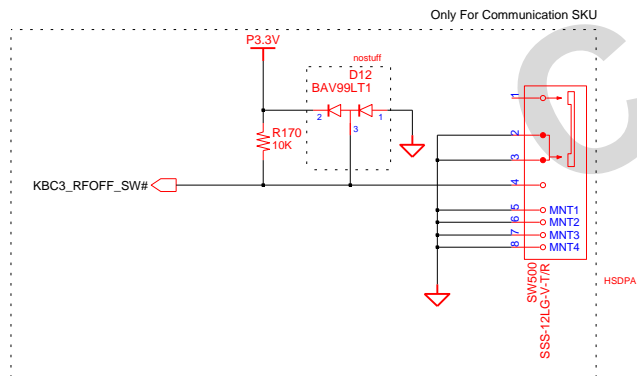
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Micom Glue Logic

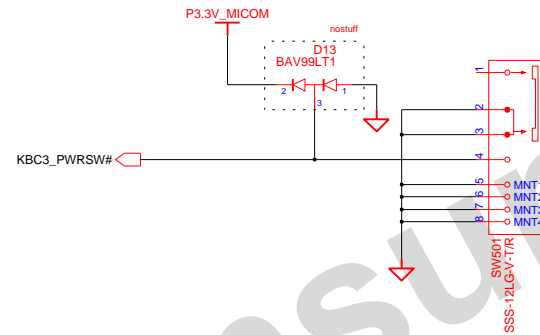
KEYBOARD



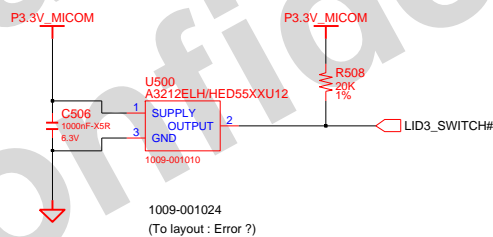
RF ON/OFF Slide Switch



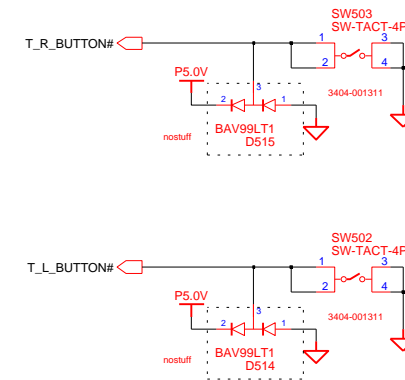
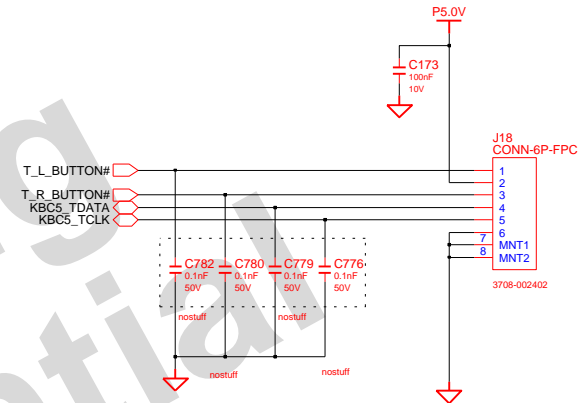
Power Slide Switch



LID_SWITCH



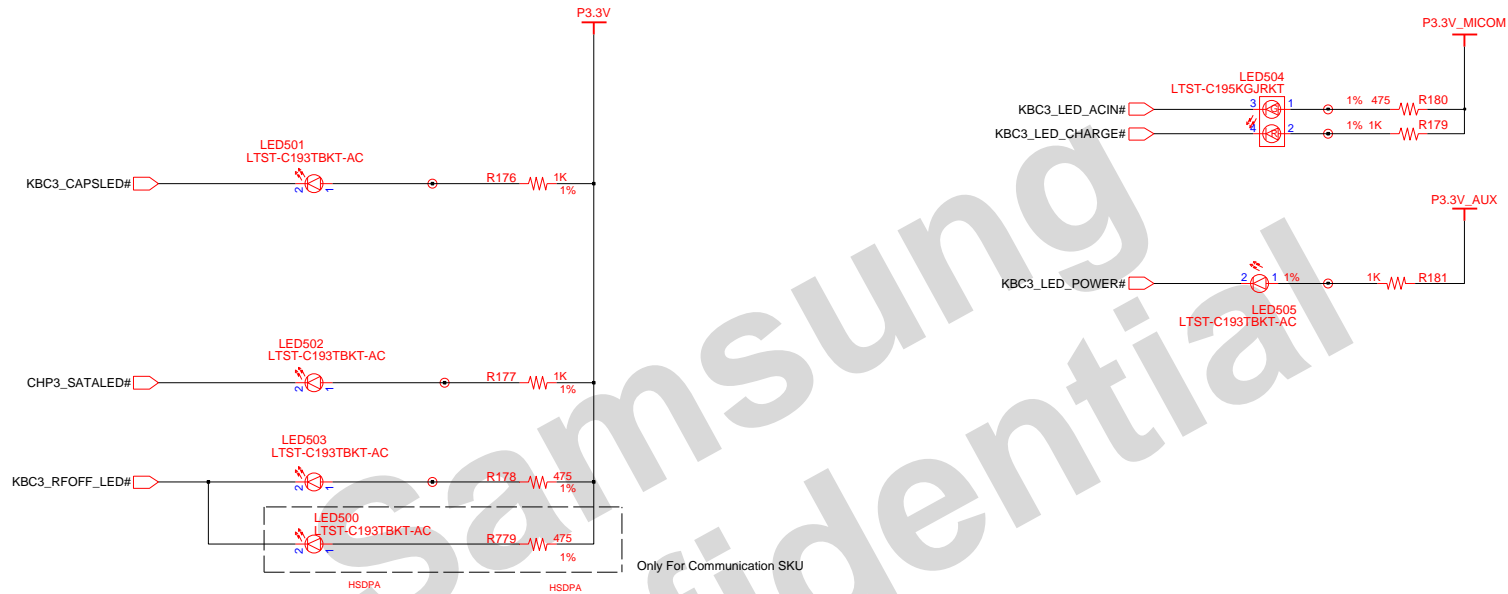
TOUCHPAD



DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON MICOM	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2		MICOM GLUE LOGIC	PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	31	OF 43

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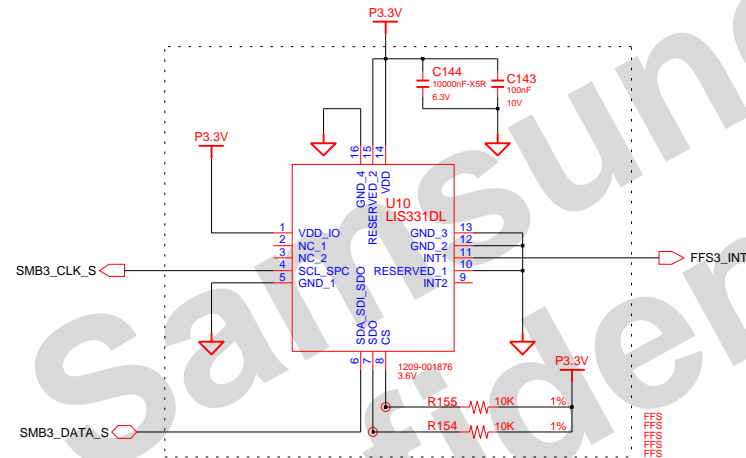
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LED SWITCH LOGIC

DRAW	BRANDON MIN	DATE	8/12/2006	TITLE	BLOOMINGTON LED_Switch	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2		LED_Switch	PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	32	OF 43

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FREE FALL SENSOR

DRAW	BRANDON MIN	DATE	8/12/2006	TITLE	BLOOMINGTON	SAMSUNG
CHECK	BK PARK	DEV. STEP	PV-2		PWR_Memory	ELECTRONICS
APPROVAL	BJ LEE	REV	0.9		PWR_Memory	PART NO. BA41-XXXXXX
MODULE CODE	undefined	LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	33	OF 43

The schematic diagram illustrates the power management circuit for the ADP3211AMNR2G integrated circuit. The IC is configured as a dual-channel DC-DC converter, providing regulated output voltages for the CPU core and various system components.

Input Section

- VCC:** Connected to the P5.0V input supply through a 6.3V capacitor (C554) and a 10kΩ pull-up resistor (R46).
- PVCC:** Connected to the P5.0V input supply through a 6.3V capacitor (C39).
- IMON:** Connected to the P5.0V input supply.
- CLKEN#:** Connected to the P3.3V input supply through a 10kΩ pull-down resistor (R47).
- VRM3_CPU_PWRGD:** Connected to the P3.3V input supply through a 10kΩ pull-down resistor (R44).
- KBC3_VRON:** Connected to the P3.3V input supply through a 10kΩ pull-down resistor (R45).
- GCORE5_PWRGD:** Connected to the P3.3V input supply through a 10kΩ pull-down resistor (R45).

CPU Core Regulator (Q5-1)

- Q5-1 (AP4232BGM-HF):** A step-down DC-DC converter used for the CPU core voltage regulation.
- FB (Feedback):** Connected to the CPU CORE output through a network of capacitors (C42, C41, C40) and resistors (R49, R50).
- COMP (Compensation):** Connected to the CPU CORE output through a capacitor (C40) and a resistor (R49).
- FRTN (Fault Return):** Connected to the CPU CORE output through a resistor (R49).
- CSREF (Current Sense Reference):** Connected to the CPU CORE output through a resistor (R57).
- CSFB (Current Sense Feedback):** Connected to the CPU CORE output through a resistor (R54).
- ILIM (Inrush Limit):** Connected to the CPU CORE output through a resistor (R55).
- LIN (Load Inductor):** Connected to the CPU CORE output through a resistor (R54).
- CSFB (Current Sense Feedback):** Connected to the CPU CORE output through a resistor (R54).
- CSREF (Current Sense Reference):** Connected to the CPU CORE output through a resistor (R57).
- CSFB (Current Sense Feedback):** Connected to the CPU CORE output through a resistor (R54).
- CSREF (Current Sense Reference):** Connected to the CPU CORE output through a resistor (R57).

GPU Regulator (Q5-2)

- Q5-2 (AP4232BGM-HF):** A step-down DC-DC converter used for the GPU voltage regulation.
- FB (Feedback):** Connected to the GPU output through a network of capacitors (C42, C41, C40) and resistors (R49, R50).
- COMP (Compensation):** Connected to the GPU output through a capacitor (C40) and a resistor (R49).
- FRTN (Fault Return):** Connected to the GPU output through a resistor (R49).
- CSREF (Current Sense Reference):** Connected to the GPU output through a resistor (R57).
- CSFB (Current Sense Feedback):** Connected to the GPU output through a resistor (R54).
- ILIM (Inrush Limit):** Connected to the GPU output through a resistor (R55).
- LIN (Load Inductor):** Connected to the GPU output through a resistor (R54).
- CSFB (Current Sense Feedback):** Connected to the GPU output through a resistor (R54).
- CSREF (Current Sense Reference):** Connected to the GPU output through a resistor (R57).
- CSFB (Current Sense Feedback):** Connected to the GPU output through a resistor (R54).
- CSREF (Current Sense Reference):** Connected to the GPU output through a resistor (R57).

Other Components

- R583, R561:** Resistors connected to the CPU CORE output.
- R584:** Resistor connected to the CPU CORE output.
- R567, R566:** Resistors connected to the CPU CORE output.
- R52, R58, R56:** Resistors connected to the CPU CORE output.
- R53:** Resistor connected to the CPU CORE output.
- R57:** Resistor connected to the CPU CORE output.
- R54:** Resistor connected to the CPU CORE output.
- R55:** Resistor connected to the CPU CORE output.
- R50:** Resistor connected to the CPU CORE output.
- R49:** Resistor connected to the CPU CORE output.
- R48:** Resistor connected to the CPU CORE output.
- R47:** Resistor connected to the CPU CORE output.
- R46:** Resistor connected to the CPU CORE output.
- R45:** Resistor connected to the CPU CORE output.
- R44:** Resistor connected to the CPU CORE output.
- R43:** Resistor connected to the CPU CORE output.
- R42:** Resistor connected to the CPU CORE output.
- R41:** Resistor connected to the CPU CORE output.
- R40:** Resistor connected to the CPU CORE output.
- R39:** Resistor connected to the CPU CORE output.
- R38:** Resistor connected to the CPU CORE output.
- R37:** Resistor connected to the CPU CORE output.
- R36:** Resistor connected to the CPU CORE output.
- R35:** Resistor connected to the CPU CORE output.
- R34:** Resistor connected to the CPU CORE output.
- R33:** Resistor connected to the CPU CORE output.
- R32:** Resistor connected to the CPU CORE output.
- R31:** Resistor connected to the CPU CORE output.
- R30:** Resistor connected to the CPU CORE output.
- R29:** Resistor connected to the CPU CORE output.
- R28:** Resistor connected to the CPU CORE output.
- R27:** Resistor connected to the CPU CORE output.
- R26:** Resistor connected to the CPU CORE output.
- R25:** Resistor connected to the CPU CORE output.
- R24:** Resistor connected to the CPU CORE output.
- R23:** Resistor connected to the CPU CORE output.
- R22:** Resistor connected to the CPU CORE output.
- R21:** Resistor connected to the CPU CORE output.
- R20:** Resistor connected to the CPU CORE output.
- R19:** Resistor connected to the CPU CORE output.
- R18:** Resistor connected to the CPU CORE output.
- R17:** Resistor connected to the CPU CORE output.
- R16:** Resistor connected to the CPU CORE output.
- R15:** Resistor connected to the CPU CORE output.
- R14:** Resistor connected to the CPU CORE output.
- R13:** Resistor connected to the CPU CORE output.
- R12:** Resistor connected to the CPU CORE output.
- R11:** Resistor connected to the CPU CORE output.
- R10:** Resistor connected to the CPU CORE output.
- R9:** Resistor connected to the CPU CORE output.
- R8:** Resistor connected to the CPU CORE output.
- R7:** Resistor connected to the CPU CORE output.
- R6:** Resistor connected to the CPU CORE output.
- R5:** Resistor connected to the CPU CORE output.
- R4:** Resistor connected to the CPU CORE output.
- R3:** Resistor connected to the CPU CORE output.
- R2:** Resistor connected to the CPU CORE output.
- R1:** Resistor connected to the CPU CORE output.

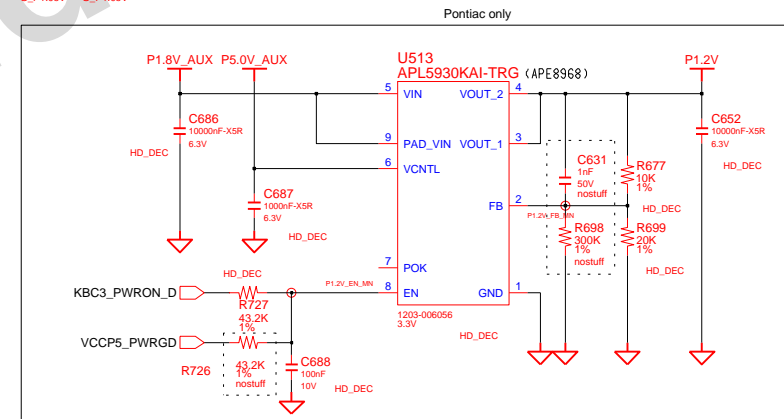
COM-22C-015(1996.6.5) REV. 3

The schematic diagram illustrates the power management section of the SAM9G45 SoC, centered around the U504 APW7141QAI TRG regulator. The regulator is configured to output P1.05V (4A) from a P5.0V_AUX input. Key components and connections include:

- Input Section:** P5.0V_AUX is filtered by R557 (10Ω) and C547 (1000nF-XSR, 6.3V). A 300ohm@TPSS1117 is connected to the input. The input is also connected to G_P1.05V.
- Regulator Pins:**
 - EN (1):** Connected to P1.05V_EN_RRRD_MN (75V) through R561 (20K) and R559 (30K).
 - OCSET (11):** Connected to P1.05V_OCSET_MN (5V) through R581 (11.8K).
 - FB (5):** Connected to P1.05V_FB_MN (5V) through R555 (17.4K) and R556 (47K).
 - Thermal (15):** Connected to 1203-006049 5V.
- Output Section:** The output P1.05V is filtered by C548 (100nF, 10V) and C526 (0.1nF, 50V, nostuff). The output is connected to G_P1.05V.
- Control and Monitoring:**
 - PGND (8):** Connected to G_P1.05V.
 - PHASE (12):** Connected to P1.05V_PHASE_MN.
 - BOOT (14):** Connected to P1.05V_BOOT_MN.
 - UVLO (13):** Connected to P1.05V_TON_MN.
- EMI Filtering:** A blue box labeled "FOR EMI" contains C70 (1nF, 50V) and C71 (4700nF-XSR, 25V).
- Other Components:**
 - C558 (100nF, 25V):** Connected to P1.05V_TON_MN.
 - R558 (200K, 1%):** Connected to P1.05V_BOOT_MN.
 - R559 (30K, 1%):** Connected to P1.05V_OCSET_MN.
 - R561 (20K, 1%):** Connected to P1.05V_EN_RRRD_MN.
 - R581 (11.8K, 1%):** Connected to P1.05V_OCSET_MN.
 - R555 (17.4K, 1%):** Connected to P1.05V_FB_MN.
 - R556 (47K, 1%):** Connected to P1.05V_FB_MN.
 - R557 (10Ω):** Connected to P5.0V_AUX.
 - R554 (100K, 1%):** Connected to P5.0V_AUX.
 - R559 (30K, 1%):** Connected to P1.05V_OCSET_MN.
 - R581 (11.8K, 1%):** Connected to P1.05V_OCSET_MN.
 - R555 (17.4K, 1%):** Connected to P1.05V_FB_MN.
 - R556 (47K, 1%):** Connected to P1.05V_FB_MN.
 - R557 (10Ω):** Connected to P5.0V_AUX.
 - R554 (100K, 1%):** Connected to P5.0V_AUX.

The regulator is configured with the following settings:

- RdsOn:** 32mohmMAX
- SET:** 1.055V
- OC:** 5.4A@32mohm, 6.7A@26mohm



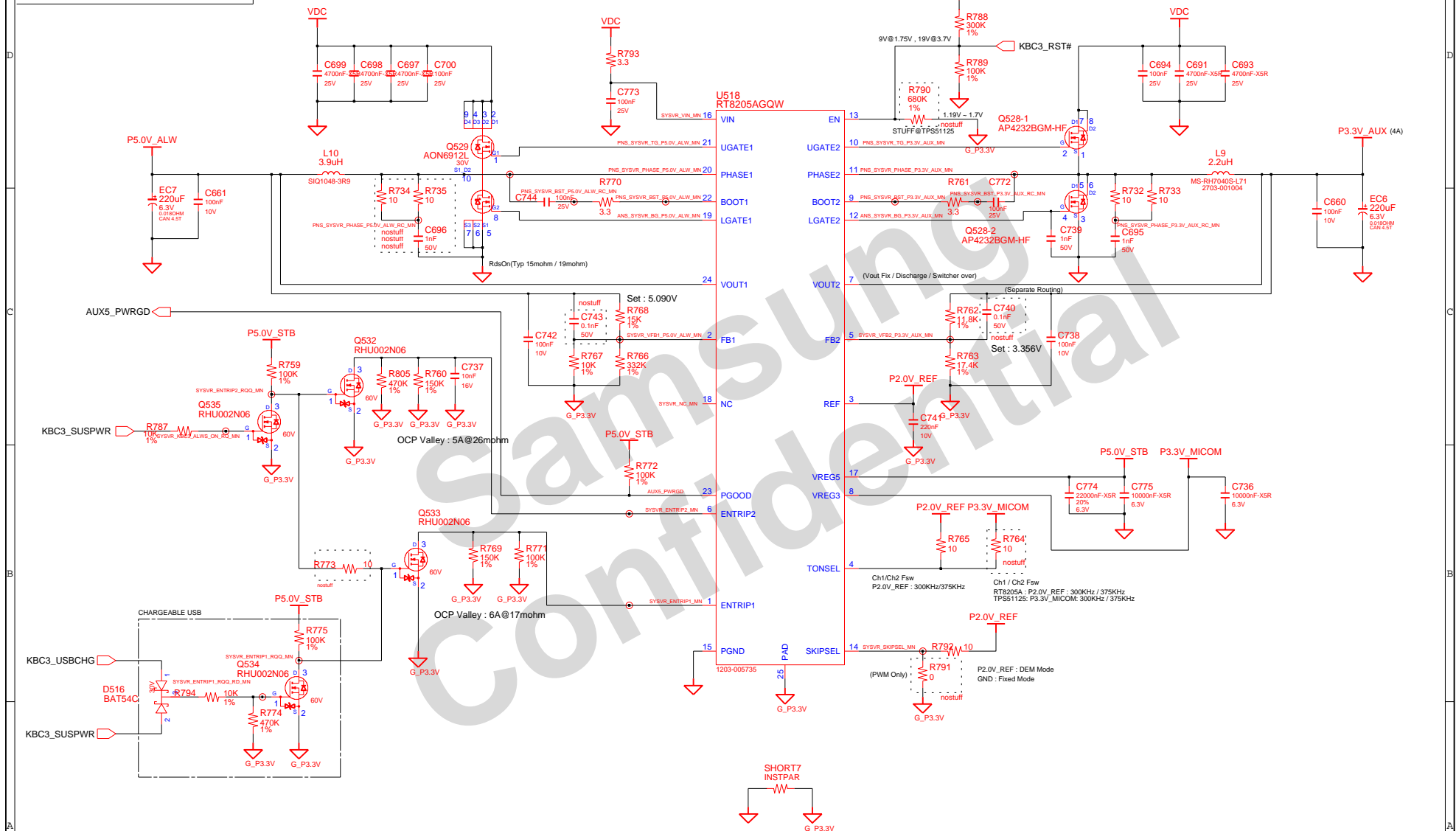
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CHECK	BK PARK	DEV. STEP	PV-2	Chipset Power		ELECTRONICS		
APPROVAL	BJ LEE	REV	0.9	P1.05V / P1.2V /P1.5V		PART NO.	BA14-XXXXXX	
MODULE CODE	undefined	LAST EDIT	October 31, 2009 11:50:03 AM			PAGE	35	OF 43

[illegible]

DRAW BRANDON MIN		DATE 01/08/2009	TITLE BLOOMINGTON PWR_Memory P1.8V_AUX		SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX	
CHECK BK PARK		REV. STEP PV-2				
APPROVAL BJ LEE		REV 0.9				
MODULE CODE undefined		LAST EDIT October 31, 2009 11:50:03 AM				

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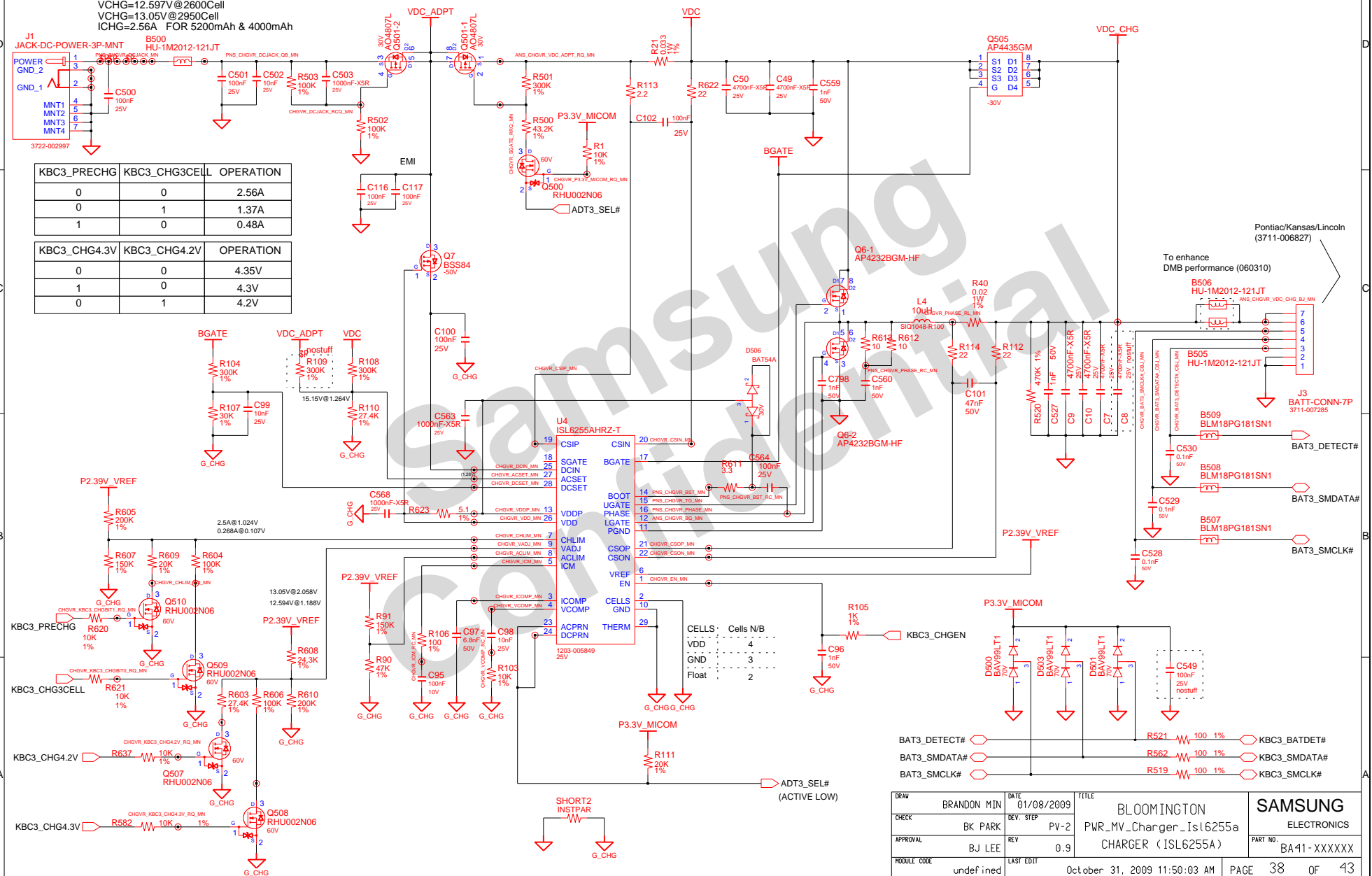
P3.3V_AUX & P5.0V_ALW

DRAW	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON PWR_MV_3V_5V	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			
APPROVAL	BJ LEE	REV	0.9		P3.3V_AUX / P5.0V_AUX	PART NO. BA41-XXXXXX
MODULE CODE	undefined	LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	37	OF 43

VCHG=12.597V@2600Cell
VCHG=13.05V@2950Cell
ICHG=2.56A FOR 5200mAh & 4000mAh

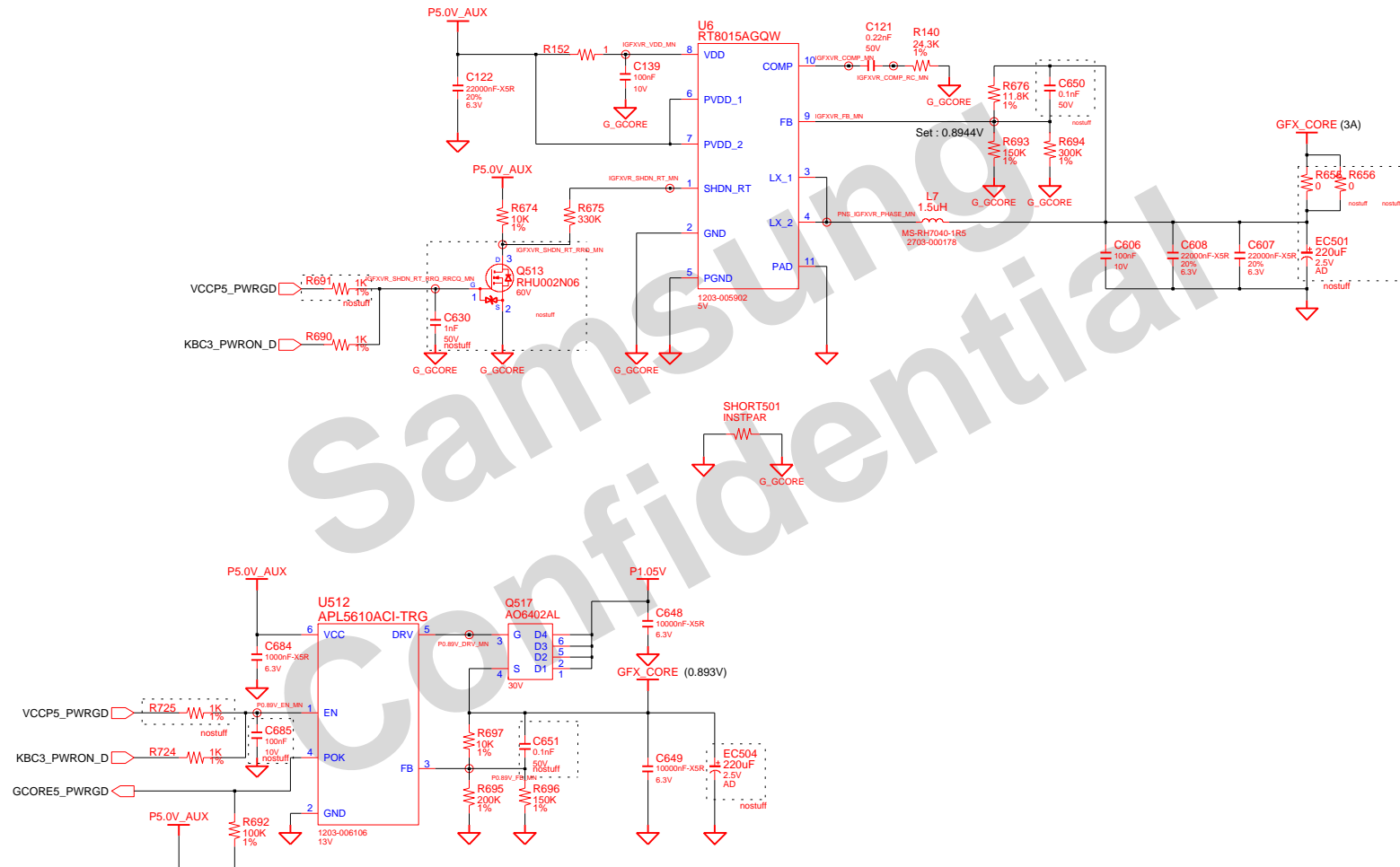
KBC3_PRECHG	KBC3_CHG3CELL	OPERATION
0	0	2.56A
0	1	1.37A
1	0	0.48A

KBC3_CHG4.3V	KBC3_CHG4.2V	OPERATION
0	0	4.35V
1	0	4.3V
0	1	4.2V



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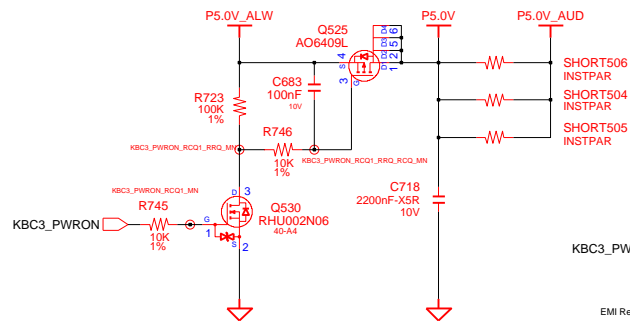
Graphic Core PWR (0.89V)

DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON INT GFX POWER 0.89V	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	39	OF 43

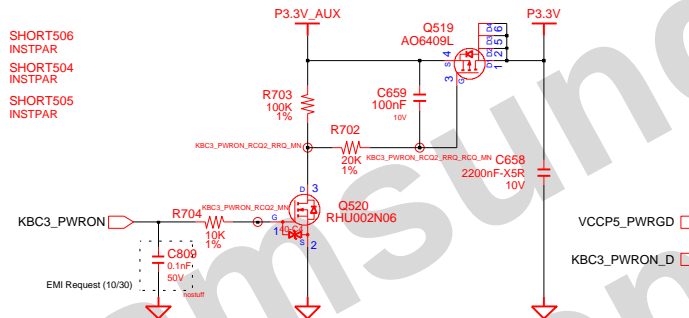
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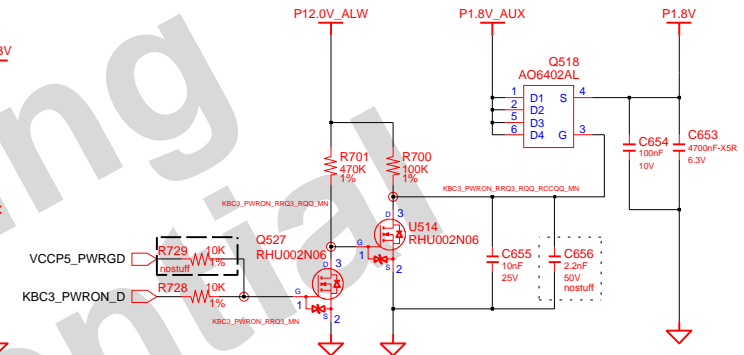
Load Switch Control (P5.0V)



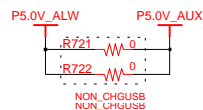
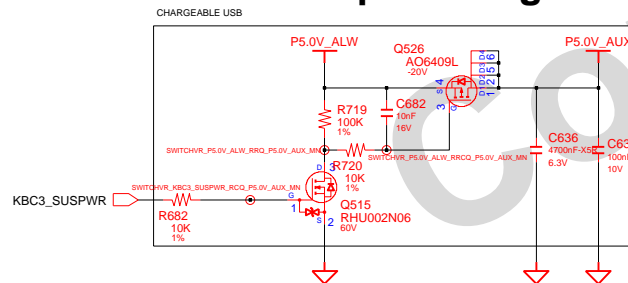
Load Switch Control (P3.3V)



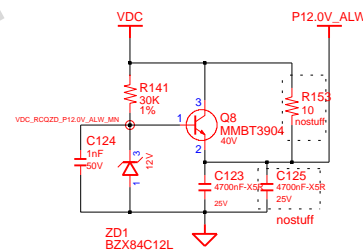
Load Switch Control (P1.8V)



Sleep'n Charger



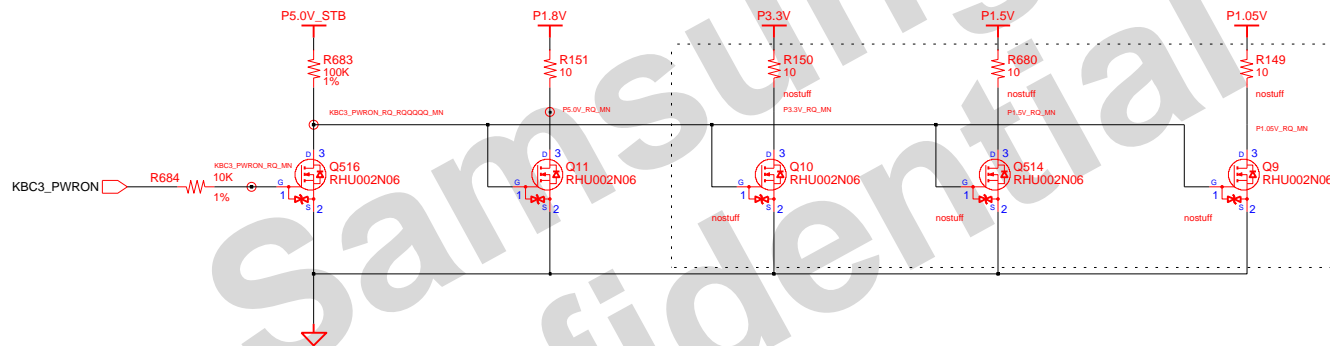
P12V_ALW



DESIGN	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON	SAMSUNG
CHECK	BK PARK	DEV. STEP	PV-2		Switched PWR	ELECTRONICS
APPROVAL	BJ LEE	REV	0.9		Switched PWR	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	40	OF 43

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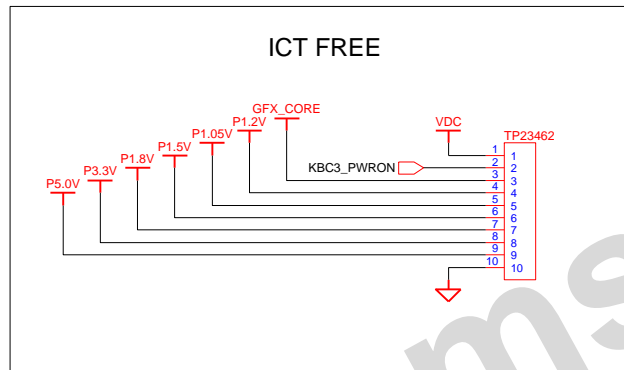
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PWR Discharger

DRW	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON Discharger	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			
APPROVAL	BJ LEE	REV	0.9		Discharger	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	41	OF 43

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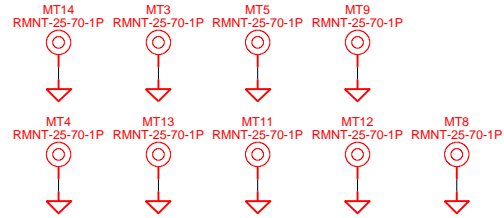
DESIGN	BRANDON MIN	DATE	3/2/2009	TITLE	BLOOMINGTON TP	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2		ITP FREE	PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	42	OF 43

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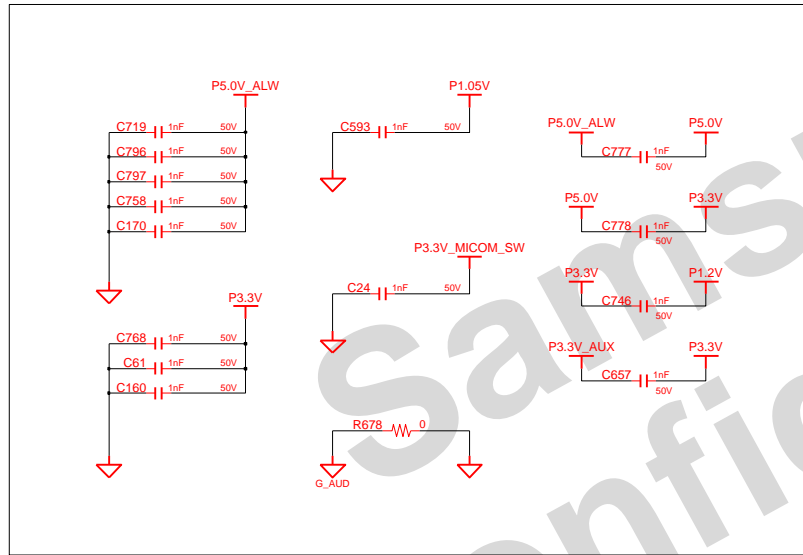
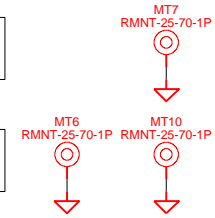
**M/B
+
Bottom**

KBD

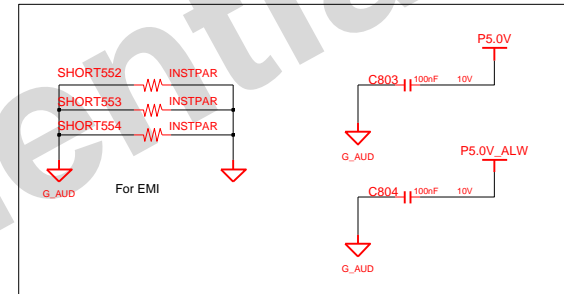
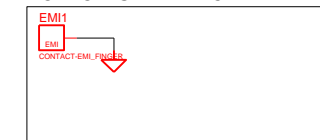


**Top + Bottom
(Bottom side)**

**Top + Bottom
(Topside)**



FOR EMI (09/25)

**BOTTOM SIDE EMI CLIP**

DRAW	BRANDON MIN	DATE	01/08/2009	TITLE	BLOOMINGTON TP ETC	SAMSUNG ELECTRONICS
CHECK	BK PARK	DEV. STEP	PV-2			PART NO. BA41-XXXXXX
APPROVAL	BJ LEE	REV	0.9			
MODULE CODE		LAST EDIT	October 31, 2009 11:50:03 AM	PAGE	43	OF 43

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500
1 O
2 O O3